SINGLE MASK, MULTIPLE LEVEL
SINGLE CRYSTAL SILICON PROCESSES:
MEMS OUT-OF-PLANE ACTUATORS
AND 3-D WIRE ARRAYS

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by
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A multilevel process and a wire process have been developed in single crystal silicon with applications in Micro ElectroMechanical Systems (MEMS). Both processes use a single mask level and can be combined with high aspect ratio bulk micromachining methods such as SCREAM (Single Crystal Reactive Etching and Metallization). The multilevel process is used to design and fabricate a micro-mirror device with a resonance frequency of 50 kHz and 20° tilt about a torsional axis. Applications of the wire process include three-dimensional photonic bandgap structures, mechanical oscillators, three-dimensional fluid channel arrays and three-dimensional arrays of self aligned lateral tips.

The multilevel process uses thermal oxidation to place structures with differing line widths on different levels without requirements of self-alignment. Structures with similar line widths are copied on to a lower level in a self-aligned fashion. The out-of-plane (Z) asymmetry created by this process is used to make a Z directional actuator. Total overlap Z drives employ a simple process but they have poor force and displacement characteristics and are shown to work for small displacements. Partial overlap drives are true Z comb drives and employ an innovative extension to the basic multilevel process. While detailed fabrication results are presented, motion is not proven on these actuators.
A micro-mirror device is designed using the partial overlap Z drive concept. Electromechanical design, process design and fabrication results are described along with relevant trade-offs. The device has not shown any movement for lack of reliable back side alignment.

The single crystal silicon wire process uses deposition-etch cycling in deep silicon etching to create released wires in each cycle. Large 3-D arrays of wires are demonstrated using this process. An alternative method of making wires using thermal oxidation is also presented. Wires less than 100nm in size and arrays as large as 9000 wires are shown. Three-dimensional cubic and hexagonal arrays have been demonstrated.

Finally, it is proposed that the multilevel and wire processes can be combined to create a stepping actuator in the Z direction.
BIOGRAPHICAL SKETCH

K. Subramanian was born in Bombay in the west coast of central India in 1974. After a short stay with his grandparents, he moved to Podanur in the south where his father was working for the Indian Railways. In 1979, he started formal schooling and moved to Madras in the southeastern coast of India, home to the second longest beach in the world. This also coincided with the birth of a baby brother in Palakkad, Kerala, who is working on his PhD at UC Berkeley at this time. The next twelve years were spent schooling at Chinmaya Vidyalaya where he topped the class almost every year and was a personal favourite of the teachers. After graduating from high school in 1991, he took the Joint Entrance Examination for the Indian Institutes of Technology, reputed to be the best and the most difficult undergraduate admission test in the world. After having made it into the top 2500 or so in the country, he enrolled in Civil Engineering and later moved to Mechanical Engineering, despite his father’s aspirations of a medical career for his son. The American bug bit him in 1993 when he saw his older friends doing interesting research abroad. A successful project in robotics and vision systems and an excellent GPA set the path to Cornell University in 1995. Working in materials processing for a year, he found out about Micro ElectroMechanical Systems in a Scientific American article during the fall of 1995. This got him into Prof. Noel C. MacDonald’s research group, where he changed his major to Electrical and Computer Engineering. The years at Cornell helped shape him into a confident and outgoing person and helped him discover several of his current interests, including travel, cooking, music and philosophy. He followed his advisor to UC Santa Barbara in 2000. In August 2001, he married the most beautiful, talented and encouraging Vidya. Several trips to Ithaca and Stanford, a few patents and a lot of late nights and weekends later, he finally decided to defend his thesis and enter the real world.
To Vidya, Rahul, Appa & Amma
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1.1 Micromachining Technologies

Processing technologies for MicroElectroMechanical Systems or MEMS in silicon have traditionally been divided into two major categories, surface micromachining and bulk micromachining.

Surface micromachining draws on the vast knowledge base available for conventional silicon processing and uses thin film deposition, patterning and etching. Structural materials include polysilicon [1] and metals such as tungsten [2]. These materials are deposited on the silicon substrate and patterned to form the MEMS structure. Structures are commonly released with a sacrificial film. As the structural films are usually thin, aspect ratio, defined as the ratio of in-plane line width to the out-of-plane depth, is very small. Mechanical structures designed for in-plane motion are hence not very rigid against out-of-plane modes. The biggest advantages of surface micromachining are versatility in processing and scaling and integration with on-chip electronics. Multiple level interconnected structures are easily made using deposition techniques and mask levels. Patterning across levels is easy as step heights are small. Thin film stresses and stiction issues are other drawbacks of this technology.

Bulk micromachined silicon MEMS uses the bulk silicon on the wafer to make a monolithic single crystal silicon structure that is several orders of magnitude stronger than surface micromachined devices. Crystal orientation dependent wet release
techniques [3] are used for lower aspect ratios while dry RIE based etches result in more controllable, larger devices with very high aspect ratios. These features give the flexibility of large mass, high stiffness, large force and high frequency motion including the ability to separate different frequency modes. Processing techniques for bulk micromachined MEMS are in many ways not as well developed as surface micromachined MEMS because large step heights limit the use of multiple masks. The root of this problem arises because a true three dimensional device can never be made from a single two dimensional lithographic pattern. One positive offshoot of these issues has led to the development of bulk micromachined devices that have no sliding parts. All motion is usually achieved using flexure thus avoiding issues like sliding friction, wear and tear resulting in superior reliability.

Aspect ratio limitations in surface micromachined MEMS have been addressed by other processes such as LIGA [4] and Hexsil [5]. LIGA employs thick resist patterning along with electroplating to fill molds. The Hexsil process uses a mold with a silicon dioxide sacrificial layer to form polysilicon structures that are released by removing the silicon dioxide film.

The 1990s saw the advent of the Single Crystal Reactive Etching and Metallization (SCREAM) [6-7] process. The ISLO [8-10] and COMBAT [11] processes are precursors of SCREAM. ISLO stands for Isolated Islands of Submicron-Silicon by Selective Lateral Oxidation and is used for the fabrication of single crystal silicon (SCS) islands on an insulating thermal silicon oxide layer. COMBAT stands for Cantilevers by Oxidation for Mechanical Beams And Tips. The process involves removing the oxide film under the SOI islands created by ISLO using a wet etch step.
SCREAM produces single mask, high aspect ratio, electrically isolated structures and is a very simple and versatile process for bulk micromachined MEMS. The evolution of the SCREAM process, extensions the basic process and advanced isolation techniques are described in the literature [12].

1.2 The SCRM process

SCREAM is a single mask process for high aspect ratio structures in bulk silicon. Devices suspended on different anchors are electrically isolated. Electrical isolation is achieved by post release metallization. A typical released SCREAM MEMS device is shown in Figure 1.1.

Figure 1.1 Released SCREAM MEMS
The spring suspends the moving structures and provides electrical contact to these structures. Fixed structures are either suspended or attached to the substrate. They are connected to bonding pads that are isolated from the moving structures. The bonding pads provide mechanical support and electrical contact. Honeycomb structures are commonly used in SCREAM devices so that suspended structures with different effective line widths can be released simultaneously.

The simplest version of the SCREAM process is shown in Figure 1.2 using ATHENA simulations. ATHENA is a process simulator and enables simulation of lithography, deposition, etching and oxidation steps among others. ATHENA simulations used for the SCREAM process are described in Appendix A. Mask oxide is either deposited (PECVD) or grown (thermal) on a silicon wafer. The oxide is coated with photoresist and a pattern is exposed on the resist. The one line pattern shown in the figure is etched into the oxide as shown in Figure 1.2 (a). The resist is stripped and the pattern is transferred to silicon using a deep silicon anisotropic technique such as the Bosch process [13] or chlorine RIE [14-17]. Figure 1.2 (b) shows a Bosch etch simulation for the pattern transfer using the oxide mask.

The sidewalls are then passivated using silicon dioxide as in Figure 1.2 (c), using either a thin film of thermally grown oxide or conformally deposited PECVD oxide. This is followed by an anisotropic oxide etch step that clears the floor of oxide and clears an equal amount of oxide on the top (Figure 1.2 (d)). The initial masking oxide ensures that all of the oxide on the top is not lost during this stage. An isotropic SF$_6$ RIE step undercuts the silicon beam as in Figure 1.2 (e). Post release metallization produces the final SCREAM MEMS structure as in Figure 1.2 (f)
Figure 1.2    SCREAM Process ATHENA Simulation
Figure 1.2 (Continued)
The entire SCREAM process is completed with one single mask. Very high aspect ratio structures are possible because the etch depth in Figure 1.1 (b) is arbitrary and is limited only by the capabilities of the etching tool. Due to the loading effect of this etch step, care must be taken to ensure that all trench widths on the mask pattern are nearly the same in order to obtain the same etch depth throughout the device. The oxide etch step in Figure 1.1 (e) also suffers from loading issues and the thickness of the initial mask oxide depends on how much oxide in the open areas is etched away for a given etch rate in deep trenches. An optional extension step after this step helps in the subsequent release. Loading effects in release are not much of a problem as long as the SF$_6$ plasma is able to enter small voids in the structure. Aluminum sputtering is commonly done for the metallization step. Sputtering ensures that both top surfaces and sidewalls are coated with metal. Post passivation, post release metallization means that the metal on the structure does not have an electrical path to the floor, to the silicon core of the beam or to neighboring released lines. The only electrical path is to the anchor from which the line is suspended. This achieves a basic form of electrical isolation and is sufficient for simple applications such as one-dimensional comb drives. Further methods to achieve more versatile forms of electrical isolation are possible using additional mask levels [18-19].

1.3 SCREAM: Scope for improvement

SCREAM has been a pioneering process for single mask SCS MEMS with electrical isolation. One of its main drawbacks, though, is that it involves a straight RIE etch when the pattern is transferred from the oxide mask into the bulk silicon. Given the physical limitation of a two dimensional mask layout, a prismatic pattern transfer
ensures that the same 2-D CAD layout is maintained across all cross sections parallel to the plane of the wafer. This concept fundamentally limits single mask devices with three-dimensional variations on the mechanical structures. Interesting variations can be obtained by controlling the device geometry in the third dimension perpendicular to the exposed pattern. Mechanical devices have traditionally had complex geometries and there is a lot of value to being able to replicate such geometries on the microscale with standard bulk micromachining technology giving the other advantages of high aspect ratio and strength.

One of the technologies presented in this thesis uses 2-D pattern geometry and thermal oxidation to create pseudo 3-D bulk structures in silicon. The other technology in this thesis uses an extreme case of profile control for the deep RIE process to create a pseudo 3-D change. The mask pattern is two-dimensional after all and structures derived from such a pattern can never truly be processed in three dimensions with a single mask.

1.4 The single mask SCS Multilevel process

Multilevel extensions to SCREAM have been demonstrated using shadow masking techniques combined with thermal oxidation [20-21]. A unique extension to multilevel SCREAM is presented here, that creates multiple silicon levels on a MEMS device by translating width information on the pattern into level information in the mechanical structure using only a single mask. Thermal oxidation is used to selectively oxidize through lines of smaller width and the wider lines thus formed are placed on a lower level in subsequent processing. The out-of-plane (Z) asymmetries
that naturally occur in this process are used to make an actuator that moves in and out of the wafer plane. A total overlap Z actuator is fabricated and is shown to work for small displacements on the order of half the difference in height between levels. Extensions to this process in combination with shadow masking are used to design a true partial overlap Z directional comb drive that can produce a constant force profile and large displacement comparable with in plane comb drives. The process is applied to a micromirror device to fabricate a mirror mounted on a torsion spring for possible optical display and switching applications. Z motion has not yet been demonstrated in the partial overlap micromirror device for lack of good back side alignment.

1.5 The single mask SCS Wire process

In yet another enhancement to bulk micromachined MEMS, very large three-dimensional arrays of micrometer to nanometer scaled SCS wires are created using a single mask and either two or three processing steps depending on process requirements. The wire process is used to create large 3-D cubic and hexagonal lattices. Process parameters and their effect on wire geometry are discussed. The wires can be integrated with SCREAM MEMS, all in one mask. Potential applications include photonic bandgap structures, mechanical coupled oscillators, particle sieves, 3-D arrays of fluid channels, piezo sensor arrays and arrays or self-aligned lateral tips.
1.6 Stepping electrostatic actuators

Standard comb fingers can be geometrically segmented to create states of higher stability in the displacement profile. These preferred states are used for stepping the comb drive to make it snap to these states for values of voltage around that state. Simulations proving comb drive stepping action are demonstrated and a process for Z directional comb drives is presented for potential future work. The process combines concepts for multilevel MEMS and wire arrays.

1.7 Outline of the thesis

This thesis is divided into three major sections. The first section describes the single mask SCS multilevel process. A basic multilevel process is presented with a proof of concept out-of-plane actuator. Process enhancements show the fabrication of a true out-of-plane comb drive with its application to a large displacement, high frequency micromirror device. Detailed design and processing results for the micromirror device are presented. The second section describes the wire process in full detail with design and processing issues and integration with SCREAM. A short third section introduces stepping actuators and describes a method to combine the multilevel and wire process to create an out-of-plane stepping actuator.
References


2.1 Introduction

A new process has been developed to produce mechanical structures of multiple levels on a silicon substrate [1-2]. High aspect ratio structures can be fabricated in single crystal silicon at multiple levels with a single lithography step and without alignment requirements. Any required difference in height between levels is defined precisely at intermediate etch steps. One application of this process utilizes the out-of-plane asymmetries produced by the multiple levels to create a total overlap out-of-plane actuator. Total overlap actuators have the movable fingers entirely inside the fixed finger system. They present a simple and basic form of out-of-plane actuation. However, the force quickly falls off with displacement compared to the constant force profile in partial overlap comb drives. Their range of motion is only half that of partial overlap drives.

2.2 Background

Several process technologies exist for the fabrication of high-aspect-ratio, single crystal silicon mechanical structures with more than one level [3-6, 11]. These processes usually involve SOI wafers, wafer bonding techniques or require self
aligned levels [9]. Figure 2.1 illustrates a sample of the different methods available for making multiple level bulk MEMS structures.

Figure 2.1 (a) shows prismatic deep etching where cross sections A-A, B-B and C-C are exactly the same and resemble the initial mask pattern. There is no geometry variation in the third dimension. Figure 2.1 (b) shows a two mask process where
multiple levels are first patterned using one mask and a second mask is used to pattern across these levels. Thick resist is required to conformally coat large steps. In addition to this being a multiple mask process, fine features cannot be patterned through very thick resist with a large depth of focus. Wafer bonding is a common technique as shown in Figure 2.1 (c). This approach also requires multiple masks. Good wafer to wafer alignment is required and processing has to be done on two separate wafers thus increasing costs. Shadow masking is shown in Figure 2.1 (d) and is a very useful technique in bulk MEMS. The physical location of a released beam is used as a mask for a lower level beam. The lower level is self aligned to the top level. By its nature, shadow masking implies that the bottom level is an exact geometrical copy of the top level. This method does not permit variations in geometry across levels.

The process described in this chapter enables fabrication of high aspect ratio MEMS structures across multiple levels on a single silicon wafer with only one lithography step and without requirements of self-alignment or shadow masking. Since only one lithography step is necessary, it is not necessary to pattern photoresist across multiple levels. Standard dry bulk processing involves deep etching of an exposed pattern and this results in structures that are essentially prismatic i.e., all cross sections parallel to the plane of the wafer are similar. This process uses thermal oxidation as a general way to change cross sections and specifically, to produce multiple levels.

Height differences leading to multiple levels are defined by a combination of line widths on the exposed pattern, etch depths during the deep RIE steps in the process and precisely controled thermal oxidation times. It is relatively simple to create two level structures given lines of different widths. If a specified relationship between line
widths is maintained, the same procedure can be extended to a larger number of levels. However, the technique extended to a very large number of levels might not be practical for certain patterns, given the constraints it will impose on the initial lithography.

The process has been used to make an out-of-plane comb actuator. Methods have been presented before for out-of-plane (Z directional) actuation [3-6], but large displacements on the order of several microns have always been a problem due to the nature of the process and the actuation mechanism. This process produces high aspect ratio Z directional actuators with displacements of a few microns to several tens of microns. Higher forces and better linearity can be achieved compared to previous methods. Such large displacements are achieved by creating large enough out-of-plane asymmetries between two levels in the silicon substrate. These asymmetries lead to forces which bring the system to an equilibrium position where the fields are symmetric.

2.3 Process Description

2.3.1 Two Level Process

A partial process sequence for fabricating two level structures is shown in Figure 2.2, which illustrates the process. The pattern exposed during lithography has adjacent lines of different widths. The pattern is transferred to the oxide using CHF$_3$ RIE. A
vertical RIE etch is used to create silicon pillars with a height equal to the required separation between levels (Figure 2.2 (a): Pillars after silicon etch). The wafer is then thermally oxidized for a time such that the thinner beams are fully oxidized while the thicker beams have a core of silicon covered by an oxide cap (Figure 2.2 (b): Oxidized Pillars). CHF₃ RIE is again used to anisotropically etch the oxide to expose the silicon floor (Figure 2.2 (c): Pillars after floor clear). The silicon is etched deeper into the substrate using RIE as in Figure 2.2 (d) and the beams are finally released with SF₆ RIE (not shown in figure). After release, the silicon dioxide can either be left in place or removed to expose the silicon beams. In either case, it is apparent that there is a two level silicon core. If silicon is used as the conducting material, the oxide need not be removed to create an electrical difference in levels. In fact, in capacitive applications, the presence of the dielectric will enhance the field when silicon electrodes are used with suitable isolation schemes.

Figure 2.2  Two Level Process Flow
For the out-of-plane (Z directional) actuator, the height difference between fixed and movable fingers that is created in this step creates a Z directional comb drive in the silicon core. In accordance with the SCREAM (Single Crystal Reactive Etching and Metallization) process [7-8], the floor is cleared, the silicon is etched down and then released with sidewall oxide protection.

2.3.2 Three Level and Multi Level Processes

The same process described above can be extended to multiple level structures. Figure 2.3 describes a process sequence for creating a 3 level structure. A pattern with three lines is transferred to silicon dioxide (Figure 2.3a) and then to silicon using deep RIE. Figure 2.3b shows three such beams of widths \( x \), \( y \) and \( z \) respectively, where \( x>y>z \). We will arrive at an approximate relation between these widths to produce a three level structure. The beams are thermally oxidized so that the thinnest beam of width \( z \) is just fully oxidized. We know that the oxide is approximately 2.27 times the volume of the consumed silicon. It follows that the widths of the silicon beams are now \( x-z \), \( y-z \) and zero and the total widths including oxide are \( x+k_1z \), \( y+k_2z \) and \( k_3z \) respectively (Figure 2.3c), as the oxidation time corresponds to a thickness of \( z \) \( \mu \)m of oxide. \( k_1 \), \( k_2 \) and \( k_3 \) are the factors that account for the increase in width corresponding to the increase in volume due to oxidation. The floor is then cleared with CHF\(_3\) RIE (Figure 2.3d) and the silicon is etched using deep RIE (Figure 2.3e). The depth of this second deep RIE step defines the difference between the second and third levels, while the first deep RIE step defines the spacing between the first and second levels as in the two level process. The lower portion of the silicon core now has widths \( x+ k_1z \), \( y+ k_2z \) and \( k_3z \). The oxide is now completely stripped from the top of the beams (Figure
A second thermal oxidation step is performed, with an oxidation time needed to fully oxidize the top of the middle beam that is $y-z$ wide. The following considerations can now be used to arrive at a relationship between $x$, $y$ and $z$ as constraints in the initial mask design for lithography:

1. When the top portion of the center beam is fully oxidized, the thinnest beam should also be fully oxidized. For a rough estimate, if we assume that the increase in volume is primarily due to increase in width, then $k_3 = 2.27$. Mathematically, we should have $y-z > 2.27z$, or $y > 3.27z$.

2. The widest beam should not be fully oxidized during the second thermal oxidation step. This means that we should have $x-z > y-z$, or $x > y$ and $x > 3.27z$, which should follow automatically from our initial assumption that $x > y > z$.

Figure 2.3g shows the three beams after the second oxidation step. The oxide on the floor is then etched with CHF3 RIE (Figure 2.3h). The third deep RIE step (Figure 2.3i) determines the height of the lowest level and the structure is finally released after sidewall oxide protection. As long as the above relations are satisfied, patterns that lie on three different levels can be made as shown in Figure 2.3i. The same process can be extended to multiple (higher than 3) levels with the oxidation and etching steps repeated in sequence. There will be several more constraints on beam widths that might play a role in the design space for the structures.
Figure 2.3 Three Level Process Flow
2.4 Processing Example: Out-of-Plane Actuator

2.4.1 Principle

Z motion, or out-of-plane actuation can be used to move stages in and out of the plane of the chip. The motions can be up and down about an equilibrium point. Small displacements out-of-plane can be achieved on high aspect ratio structures by biasing the substrate. Essentially, the presence of the substrate removes the vertical symmetry in the field lines, thus producing an out-of-plane force. This force depends on the geometry of the actuator. For a comb actuator, it depends on the spacing between fingers, the geometry of the finger and the distance to the substrate. This force is limited in range as the system reaches equilibrium very close to the starting position. The force is also fairly non-linear and a linear approximation is valid over only a very small range.

In plane comb drives work by creating an asymmetry in the electrostatic field due to an applied voltage across interdigitated fingers. The fingers move, so as to create an electromechanical equilibrium. These drives have the inherent advantage that they produce large forces and can move large distances depending on their geometry. This design can be replicated in the Z direction except for the following problem. Most standard processing methods to produce deep structures result in prismatic structures. In other words, once a two dimensional pattern is exposed on photoresist, the same pattern is etched down deep into the substrate, as a result of which any cross section parallel to the plane of the wafer would look the same. This means that asymmetries in the Z direction do not occur naturally due to deep etching and pattern transfer. Our
process can be used to create multiple levels and hence asymmetries in the Z direction. With this process, different cross sections parallel to the wafer plane would look different depending on what levels they include. The multiple levels can be created in such a way as to work in parallel to produce an upward force to move a stage.

2.4.2 Actuator Design

The actuator integrates interdigitated comb fingers at two different levels. The fixed fingers are at one level and the movable fingers are at a lower level. These fingers need to be attached to a spring that is more compliant for out-of-plane motions than in-plane motion. A torsional spring is the simplest case for such motion and is used for this purpose. The fringing fields due to an applied voltage pull the lower fingers upwards. Figure 2.4 shows the field lines that create the forces on these combs. Silicon was defined as a perfect conductor and the oxide was defined as a dielectric. The field lines shown are for an applied voltage of 1 Volt. For additional force, the substrate and the movable fingers are grounded, while the fixed fingers are positively biased. As seen in Figure 2.4, the height difference between fingers, as well as the presence of the substrate as a ground plane, both add to the vertical force.
In Figure 2.4, the center comb is thinner and has silicon only on the lower level. The top of the center comb finger is fully covered with silicon dioxide. For the fingers on either side, the top half is a core of silicon covered with silicon dioxide, while the bottom half is only silicon. The field lines on the lower level are perpendicular to the fingers and curve at the ends. The substrate helps in enhancing vertical asymmetry by diverting some of the field lines away from the actuator.
This method of actuation seems to have a higher range and better linearity compared to actuation based on the ground plane alone, with all fingers at the same level. The two cases were simulated in Coulomb, an electrostatics simulation package that uses the Boundary Element Method. Figure 2.5 shows the Force vs. Displacement graph for actuation based on the effect of the ground plane alone. The total displacement corresponds to the equilibrium position, where the force is zero. This is seen to be about 0.5 µm from the plot. Figure 2.6 shows the same plot for actuation with two level comb fingers.
Figure 2.6  Force vs. Displacement Simulations: Z Actuator with Oxide Cap

The simulation was done for a height difference of 10 μm, an applied voltage of 1V and a gap between comb fingers of 3.5 μm after oxidation. This simulation considers comb fingers 3.5 μm apart compared to only 1.5 μm in the other case that uses the effect of the ground plane only. There is still a much higher force, larger range of motion and better linearity in the case of the oxidized Z actuator with a height difference compared to ground plane based actuation. The results show a maximum displacement of more than 5 μm (Figure 2.6) when the force reaches zero. It is reasonable to expect that the maximum displacement is about half the height...
difference as the fields would balance on all sides of the moving finger at that position. This is verified in the plot, where the force goes to zero at slightly more than 5 µm. The difference is due to the presence of silicon dioxide, which enhances the stored energy in the capacitor. It can also be seen by comparing the plots that the two level Z Actuator is more linear and produces larger force than the actuator based on ground plane levitation alone.

Figure 2.7 shows a comparison of the electric field lines for the two level Z actuator between the starting position, where the upward force is the strongest and at equilibrium, where all forces are zero and the fields look symmetric.
Figure 2.7  Field lines: Starting Position (Left, Oxide Stripped),
Equilibrium (Right, Oxide Present), Oxide: Black, Silicon: Clear
2.4.3 Two Level Z Actuator Process Sequence

The Z actuators are made with the 2 level process sequence described in Section 2.3.1 and Figure 2.2. At the lithography stage, comb fingers of alternating larger and smaller widths are exposed on photoresist and the pattern is transferred to silicon dioxide using CHF₃ RIE. Figure 2.8 shows lines of 1.1 µm and 0.8 µm on oxide.

Deep RIE on the Bosch etcher is used to etch silicon using the oxide mask. A height of 10 µm in the silicon is achieved during this step. This step defines the height difference between adjacent comb fingers in the final device and corresponds to a maximum Z displacement of approximately 5 µm as discussed. The wafer is now oxidized so that the silicon in the thinner fingers is fully consumed. Figures 2.9 and 2.10 show the fingers at this stage of the process with the oxide stripped using HF.
Figure 2.9  Oxidized Comb Fingers: Oxide Stripped

Figure 2.10  Oxidized Comb Fingers: Oxide Stripped, Finger Close Up
The thicker finger shows the core of silicon, while the thinner fingers have almost completely disappeared. A spike in place of the thinner finger shows the profile of the oxidation boundary due to the presence of the corner. This spike is exposed when the oxide is stripped. Figures 2.9 and 2.10 clearly show the beginnings of a two level structure. If the oxide is not removed, it is used as a mask to etch deeper into the substrate.

In accordance with the SCREAM (Single Crystal Reactive Etching and Metallization) process [7-8], the floor is cleared and the etch is extended into silicon using deep RIE as shown in Figure 2.11.

Figure 2.11 Floor Clear and Extension Etch

The device is then released after sidewall oxide passivation and floor clear. The released structure is shown in Figure 2.12. In the figure, the movable and lower
fingers are attached to the central limb while the fixed fingers are attached to the outer limbs. It is clearly seen that the movable fingers are at a lower level, thus proving the two level process. The complete torsional actuator with the Z stage is shown in Figure 2.13. The device has been tested inside the SEM and it shows a maximum DC displacement of 4 µm at 40 V.

Figure 2.12    Torsional Z Actuator Showing 2 Level Comb Fingers
2.4.4 Isolation Requirements

The simplest isolation scheme is to strip the top level oxide and metallize the device after thin oxide is deposited or grown. The device shown in Figure 2.12 had 150nm of PECVD oxide deposited after an oxide strip. As the operation voltages are fairly low, aluminum was sputtered on the device. The fixed and moving structures are hence isolated from each other and from the substrate as in standard SCREAM.

It is possible to use the substrate silicon as a conductor in the Z motion actuator since the asymmetry exists in the silicon core. An oxide strip is not required in this case, but this mandates the use of a scheme to electrically isolate different parts of the structural
silicon, the fixed and movable fingers in particular. One such scheme is shown in Figure 2.14. There are oxidized trenches that are present on free standing beams to isolate one section of the beam from another [10]. This particular scheme becomes more difficult to implement when the aspect ratio of the device becomes higher, translating to larger out-of-plane motion capabilities in the device. This technique also requires an extra mask level to make the trenches before the Z actuator structures are fabricated.

Another scheme using wafer bonding techniques can be used if silicon is used as the conductor. One wafer is thinned down to the required structural height and the structures are fabricated on this wafer until after the high temperature thermal oxidation steps. This wafer is now bonded to a standard wafer using either oxide or photoresist. The structures are now etched through the top wafer. The support wafer either has crudely aligned trenches for release or the photoresist or oxide is isotropically etched to release the structures.
2.5 Problems and Issues with Z Actuator Total Overlap Design

The Z actuator is an excellent example of the features of the multilevel process. The actuator, however, is very simple in its current form. Looking at possible applications for out-of-plane actuation, there are several issues that might need improvement. Given that a standard in-plane comb drive probably gives the best electrostatic force and displacement for a given voltage, it is conceivable that a good Z actuator should resemble a comb drive as closely as possible. The most obvious difference between the design presented in this chapter and a true comb drive is the fact that the movable fingers totally overlap the fixed fingers, while in a true comb drive, there is only a partial overlap between the fixed and movable fingers.

More results on the Z actuator are presented here to discuss possible drawbacks of the total overlap design by studying the influence of several parameters on the force and displacement characteristics of the actuator.

2.5.1 Effect of Finger Gap

We expect intuitively that the forces and displacements should be higher for smaller finger gaps. The graph in Figure 2.15 shows a Force-Displacement plot for different finger gaps. The smaller gaps yield a larger starting force as expected, but the force also seems to fall much more rapidly, resulting in a very small displacement to equilibrium when the gaps are small. The linearity of the Force-Displacement curves is restricted to the region $0 < z < z_{\text{max}}$, where $z_{\text{max}}$ is the maximum displacement value for a certain spring stiffness. On the graph, it is the value of $z$ at the point of intersection of the Force vs. $z$ curve with the restoring force.
This is explained by the fact that the lower level of the Z actuator is wider than the upper level because of the volume expansion due to oxidation. Wider fingers at the lower level mean smaller gaps. If we think of the fixed fingers as two separate levels, there are two comb drive systems pulling on the same movable finger. The top level of the fixed fingers pulls the movable finger up while the bottom level of the fixed fingers pulls it down but more strongly compared to the top level because the gaps are smaller here, as illustrated in Figure 2.16. The width differential between the two
levels is experienced less and less by the movable finger as the gap increases. This also explains why the maximum displacements are closer together at larger gaps.

\[
F = \varepsilon \frac{b}{d},
\]

where \( F \) is the force, \( \varepsilon \) is the permittivity of the medium, \( b \) is the in plane length of the comb finger and \( d \) is the gap. For a gap of 3.5 \( \mu \)m, and a depth of 30 \( \mu \)m as used in the simulation, the force in vacuum turns out to be \( 7.6 \times 10^{-11} \) N, which is below the maximum possible force for this gap. This means that this system is inferior to a true comb drive even at the starting point. Additionally, the force falls off very fast unlike a true comb drive where the force is constant with respect to distance.
The restoring force of a sample spring overlaid on the graph reduces displacements further.

2.5.2 Effect of First RIE Etch Depth on Maximum Force

Figure 2.17 Total Overlap: Effect of first RIE etch on Starting Force

Figure 2.17 shows the effect of changing the first RIE etch depth on the maximum force for a 3.5 µm gap between fingers. It shows that the etch depth has to be at least 10 µm, beyond which the maximum force saturates. A zero etch depth means that there is no height difference between levels and the actuation is only due to the
presence of the substrate. The starting force gradually ramps up as the height difference becomes more and more significant. While this effect is in itself fairly intuitive, the downside is that picking any data point beyond saturation as the first RIE etch depth does not seem to have a significant effect on the maximum displacement as shown in Figure 2.18.

![Effect of RIE1 on Force & Displacement](image)

**Figure 2.18 Effect of RIE1 on Force and Displacement**

This means that the theoretical maximum displacement for a Z comb drive with a 3.5 μm gap and any height difference over 10 μm will be about 6 μm only. This fact has serious implications in scaling up such a design to achieve large displacements. The
effect is again due to the fact that the lower comb drive system is much stronger than the upper system and for a given finger gap, the Z displacement goes into saturation beyond a certain value of RIE 1.

2.5.3 Effect of Lower Level RIE Etch Relative to RIE 1

Figure 2.19  Total Overlap: Effect of Lower Level RIE for 10 µm RIE 1

Figure 2.19 shows the Force – Displacement plot for different values of lower level RIE (RIE 2) for an upper level RIE or a height difference between levels of 10 µm. The starting force and maximum displacement do not seem to be affected significantly
by changing RIE 2. Figure 2.20 shows a similar plot for a 50 µm RIE 1 and this plot shows very different results compared to the 10 µm case. Linearity is restricted to the initial portion of the curves only.

![Effect of 2nd RIE Etch, RIE1 = 50µm](image)

**Figure 2.20** Total Overlap: Effect of Lower Level RIE for 50 µm RIE 1

For very low values of RIE 2 relative to RIE1, the starting force seems to be higher. It is difficult to explain this weak phenomenon. Perhaps, the system is tending towards the limit where near zero RIE 2 means very low starting force. The more significant phenomenon observed in this plot is that lower values of RIE 2 give very large values
of displacement. A close up of the region of interest is shown again in Figure 2.21 for clarity. The 2 µm and 5 µm lines reach all the way until the theoretical displacement of about 25 µm which is half of RIE 1. The 20 µm and 30 µm curves reach zero at about 7 µm displacement and turn around at approximately 20 µm and 30 µm respectively, while the 50 µm curve never turns around once it becomes negative.

![Graph showing force vs. displacement](image)

**Figure 2.21 Close Up View of Figure 2.20**

It is easy to explain this phenomenon if we reconsider the fact that the comb fingers have a smaller gap for the entire length of RIE 2. The 20 µm and 30 µm curves in the figure feel the overwhelming force of the lower level comb system and reach equilibrium at around 7 µm. However, when they cross out of that system at
displacements approximately equal to the respective RIE 2 values itself, the force picks up again and they tend to reach the 25 µm midpoint value. The 50 µm curve, however, never leaves the lower level system and hence never turns up again. For the 2 µm and 5 µm cases, it so happens that they leave the lower level comb drive system even before they reach the 7 µm equilibrium point and they travel on to the 25 µm midpoint without reaching zero force along the way.

The significance of this result is that even though the displacement saturates above certain values of RIE 1 as shown in the previous section, it is possible to reach theoretical displacements simply by tuning RIE 2 values, specifically, by reducing them. The obvious drawback is that the force falls very fast until the first equilibrium point of 7 µm, whatever RIE 2 may be. This means that the mechanical restoring force would, unfortunately, still limit the range of motion of the system.

2.5.4 Effect of In-Plane Finger Length

In-plane finger length, or the overlap length plays the same role in Z actuators as etch depth in planar comb drives. The force increases in linear proportion to the in-plane length of the fingers. Figure 2.22 shows the effect of doubling finger length on a device that was etched 100 µm RIE 1 and 5 µm RIE 2.
2.5.5 Effect of Voltage

Voltage was found to have the same effect as for regular comb drives. The force is proportional to the square of the voltage. Figure 2.23 shows that the plot of Force vs. the square of the voltage is perfectly linear.
Figure 2.23  Total Overlap: Force as a Function of Voltage Squared

2.5 Conclusions

Processes to make multiple level structures have been demonstrated successfully. The processes lend themselves to high aspect ratio bulk micromachining of single crystal silicon. Structures can be fabricated at multiple levels with a single lithography step and without alignment requirements and intermediate etch steps can define the difference in height between levels. This technique is easily combined with single level high aspect ratio MEMS processing methods.
Out-of-plane asymmetries produced by the multiple levels have been used to create a total overlap out-of-plane actuator stage with force fall-off with displacement. Thermal oxidation techniques have been used successfully in producing height differences in the Z direction. The two level process has been used to create a Z-directional comb actuator. A height difference of 10 µm between levels moves the comb fingers a distance of 4 µm in the Z direction. The dielectric covering the silicon increases the actuation force by increasing the stored energy in the capacitor system and is hence left unstripped in the device. A potential problem with leaving the oxide unstripped is increased moving mass that lowers the resonance frequency of the device. The point of equilibrium in the Z motion is at a displacement of approximately half the height difference between adjacent comb fingers. Forces and displacements are higher with the oxide present, compared to the case when the oxide is stripped. The high aspect ratio actuator created using this process is compared specifically to an actuator based on biasing the ground plane with no height difference between the fingers.

Large displacement Z motion actuators need to be made and can be combined with in-plane X and Y stages so as to create a complete three degree of freedom stage. Silicon tips have been created on high aspect ratio beams as in Figure 2.24. Such tips can be mounted on the stage so that they can move with three degrees of freedom. Figure 2.25 shows the schematic of a silicon tip mounted on a Z stage. Such a stage can be mounted within in-plane stages as shown in Figure 2.26 and Figure 2.27 with the required isolations.
Figure 2.24  Silicon Tip formed by Thermal Oxidation

Figure 2.25  Z Actuator with Silicon Tip
The innermost stage is the Z stage and can move in and out of the plane depending on which side is actuated. Note that the Z stage suspended fingers and supporting structures are thinner and hence will be lower level in the 2 level process. All other fixed and suspended fingers and frames and springs are of wider width. The next outer stage is the Y stage and can move up and down in this view. The outermost stage is the X stage and can move left and right in this view. Suitable isolation schemes are required to achieve this stage within a stage within a stage design.
Figure 2.27  XYZ Stage Within a Stage Within a Stage Design: 3-D View
The effects of various parameters on the performance of the Z actuator have been studied in detail. It is found that however large the first RIE etch, the displacement saturates at a certain point depending on the finger gap. The second RIE etch can be tuned to shift this saturation point to theoretical values. In either case, the force fall off is too fast to use the actuator for large displacement applications. The problems with force fall-off and reduced range of motion can be solved by using partial overlap Z comb drives as described in Chapter 3. Chapter 3 describes the design of these drives in detail with the idea of using them for a micromirror device. Partial overlap drives are designed for twice the range of motion compared to total overlap drives and constant force over this range.
References


3.1 Introduction

It has been shown in the preceding chapters that a simple two level process results in a comb finger system with multiple height fingers where the smaller movable fingers are totally overlapped by the taller fixed fingers. Results showed that such comb fingers are only suitable for a small range of motion because of the linear force fall off with respect to out-of-plane displacement. This rapid drop in force combined with wider lower level structures caused by thermal oxidation results in a saturation value for a maximum displacement that can be partly alleviated by controlling the second level extension etch. To create a true comb drive in the Z direction, the movable finger has to have both an overlapping and a non-overlapping portion as in the partial overlap comb drive shown in Figure 3.1. More accurately the partial overlap has to be at least electrical, if not both electrical and mechanical. This means that looking at the voltage bias alone there has to be a finite, non-zero, non-complete overlapping section where comb fingers are oppositely biased.

As is very well known for in-plane comb drives, the initial overlap of the comb fingers contributes to the starting force and ensures that the comb drive will begin to move. The non-overlapping portion of the fingers ensures that the force is constant and that the range is motion is equal to the entire length of the fixed fingers. The range of motion is defined differently here as compared to total overlap drives since the
constant force profile affords the luxury of a more strict definition. Very simply, it is defined as the range of displacements over which the force is constant. In the absence of initial overlap, the force climbs to this constant value when the movable finger enters the fixed finger gap. Once the displacement approaches the fixed finger length, the force falls off to zero to reach an equilibrium displacement that depends on the length of the movable finger. This chapter describes the design and fabrication of Z comb drives approaching such an ideal behavior.

Figure 3.1 Total and Partial Overlap Comb Drives
3.2 Three Level Shadow Masking

Shadow masking is used to create a lower level in a released MEMS structure that is a prismatic copy of the widest dimension on a top level structure. The deep RIE step is a straight silicon etch step. It can be made to use the physical location of a top level structure, or rather, the shadow of that physical location as a mask for a lower level etch instead of using a hard etch mask like photoresist or oxide. The fact that the shadow is used for masking implies that the lower level structure is as wide as the largest dimension in the top level structure because the shadow is as wide as the largest width. Shadow masking is possible with the right etch recipe as long as the out-of-plane distance between the two levels is not too large. Figure 3.2 is an example of shadow masking where the fixed fingers on the comb drive have two levels. The top level has been oxidized and has become wider than the line widths on the corresponding mask pattern. The bottom level is pure silicon with a beam width equal to the total width of the oxide and the silicon. The top level of the movable fingers has been physically removed with a probe to show the two levels clearly.

Shadow masking can be combined with the two level process to make two level and three level devices using a single mask. A device made with the two level process using line width variation and thermal oxidation can be shadow etched after release to create a third level that is a copy of the second level.
3.3 **Z Actuator with Three Level Shadow Masking**

Figure 3.3 shows a schematic of a Z actuator comb finger system that uses both the two level process and the shadow masking process to create a total of three levels.
A, B and C in Figure 3.3 are fabricated with the 2 Level Process. B is of smaller width and hence has only oxide on the top level. A and C are wider and have a silicon core with an oxide cap on the top level. After release, a shadow etch creates the third level 1,2 and 3. If B and 2 can be mechanically connected and if 1 and 3 can be electrically removed from the system, this would resemble the comb drive schematic shown in Figure 3.4 and would create a partially overlapped comb drive as desired.
Figure 3.4 Three Level Partially Overlapped Comb Fingers

1, 2, 3 & A, B, C are Electrically isolated
B-2: Mechanically Connected

Figure 3.5 Isolation Necks on Wider Lines
To achieve electrical isolation between A-1 and C-3, A and C are not fully released before shadowing. There is a small neck that remains just after C is released. This neck is then oxidized during a subsequent thermal oxidation step to create vertical isolation between the two levels of the wider fingers. The isolation neck is shown in Figure 3.5. Partial release on these necks is shown by the small oxide overhang around the neck caused by the sidewall passivation before the undercut.

The comb finger schematic in Figure 3.4 illustrates an effective electromechanical picture of the device. The fixed fingers A and C are positively biased, while their shadows 1 and 3 are grounded. Thus, 1 and 3 are nearly removed from the electrical picture. This biasing scheme is possible because A is electrically isolated from 1 through the oxide segment and so is C from 3. The exact way this is done will be made clear in the process flow in later chapters. Next, the lower level of B and its shadow 2 are grounded. Even though B and 2 are independently released, they need to be mechanically connected on the support structures away from the fingers.

In the original version of the Z actuator, A and C were positively biased, whereas B was grounded along with the base plane. The reason the model proposed here is better is that B-2 does not overlap A and C entirely. Rather, there is a portion 2 extending out from A and C.

There is one other design variant for Z drives that use the shadow masking process. The two level process in A, B and C can be stopped at the stage where thin lines are oxidized through. A release followed by a shadow etch would result in a two level structure that works as a non-overlapping comb drive rather than a partially overlapped drive. The significance of such a comb drive will be explained shortly.
Figure 3.6 shows the biasing scheme for both the two level and three level shadow masking variants. The two level variant is easier to process but suffers from a low starting force because the movable finger needs to move a few µm before it overlaps.
The advantages of the partial overlap feature are two fold:

1. The force will be constant over the entire range of motion of B-2. In the total overlap case, B-2 would completely overlap A & C and the force drops down to zero linearly.

2. The range of motion of the Z drive will be the approximately equal to the entire difference in height produced by the two level process. The required processing condition that must be met is the sum of the second and third level deep RIE etches referred to as RIE 2 and RIE 3 respectively should be greater than or equal to the first deep RIE etch, RIE 1. In the earlier case of total overlap, the range of motion was approximately half of RIE 1 and was very sensitive to RIE 2.

The electric field lines for the partial overlap configuration are shown in Figure 3.7 at the starting position. Figure 3.8 shows symmetric field lines at the equilibrium position when the actuator has moved the entire length of RIE1.
Figure 3.7  Field Lines in Three Level Shadow masked Z Actuator: Starting Position, Oxide: Black, Silicon: Clear
Figure 3.8  Field Lines in Three Level Shadow Masked Z Actuator: Equilibrium
Oxide: Black, Silicon: Clear
3.4 Vertical Gap

Post release shadow masking results in a vertical gap between the silicon levels in the device. The release etch is isotropic and the ratio of lateral etch rate to vertical etch rate in the release step depends on the chamber pressure, gas flow rate and the RIE power in the recipe. The SF₆ flow rate in the process is the maximum possible 100 sccm in the Bosch etch tool. Lower RIE power or RF power makes the release more isotropic. However, the loading effect is too high at low power because the gases cannot enter smaller etch vias.

We achieve good balance between an isotropic profile and loading, by using low pressure (13 mT), high SF₆ flow rate (100 sccm) and high power (35 W). These parameters will be discussed in greater detail in later chapters. The result of the trade off between loading effect and isotropic profile is that the vertical etch rate during the release step is higher than the lateral etch rate, thus pushing the silicon floor down. Figure 3.9 explains this phenomenon. The perfectly isotropic release in the figure has a lower vertical gap between levels compared the release profile that is less isotropic.

Vertical gap affects the starting force for a two level shadow masked comb finger. The force has to ramp up to the constant value or, equivalently, the moving finger has to overlap the fixed fingers before the spring stops the displacement. For a three level process, the vertical gap does not affect the starting force as much. The starting force is comparable to the total overlap Z drive in this case and the vertical gap appears as a slight depression in the force in the early part of the travel depending on RIE 2.
As explained earlier, vertical isolation is achieved by oxidizing through the partial undercut produced by the first release step. This undercut has to be wide enough to maintain the strength of the structure. If the undercut is too wide, the thermal oxidation step will nearly oxidize all the way through the wider lines too, which defeats the purpose of the two level process. Release time, therefore, is a function of the line widths being released, the line widths that should not be released and the size of the smallest etch vias.

Figure 3.9 Larger Vertical Gap with Less Isotropic Release

3.5 Vertical Isolation
3.6 Characteristics of Two and Three Level Z Comb Drives

3.6.1 Constant Force and Large Range

Figure 3.10 shows a constant force profile for a two level non-overlapping Z actuator. The plot is for 50 µm RIE 1, 60 µm RIE 2, comb fingers 30 µm in length and a post oxidation gap or lower level finger gap of 2.5 µm. The maximum force is \(9.37 \times 10^{-11}\) N. The force is constant from around 5 µm to 48 µm Z displacement. The vertical gap between the two levels is 3 µm and the force climbs from \(2 \times 10^{-11}\) N at the
starting point to near maximum when the movable finger overlaps the fixed fingers. The force on a standard comb finger pair per volt is given by $F = \varepsilon \frac{b}{d}$, where $F$ is the force, $\varepsilon$ is the permittivity of the medium, $b$ is the in plane length of the comb finger and $d$ is the gap. For a gap of 2.5 \( \mu \text{m} \), and a finger length of 30 \( \mu \text{m} \), the force in vacuum turns out to be $1.06 \times 10^{-10}$ N, which is almost equal to the peak force in this system. Except for the starting force, we thus have a configuration that resembles a true comb drive.

3.6.2 Effect of Finger Gap

![Graph showing the effect of finger gap on force versus displacement.](image)

**Figure 3.11**  Non-Overlapping Combs: Effect of Finger Gap
As expected, the force in the comb drive is inversely proportional to the finger gap. Figure 3.11 shows plots for lower level finger gaps of 1.5 µm, 2.5 µm and 3.5 µm. RIE 1 is 50 µm, RIE 2 is 60 µm, finger length is 30 µm and the vertical gap is 3 µm. Finger gap does not affect the range of the system. Though it is not obvious from the plot, the starting force is mildly smaller for larger gaps. The starting force at the 1.5 µm gap is $2 \times 10^{-11}$ N while the starting force at the 3.5 µm gap is $1.86 \times 10^{-11}$ N. When the comb finger starts moving, the closest fixed fingers, which are the lower level fixed fingers, are also grounded. The only field experienced by the movable finger is from the top level fixed fingers. These fingers are quite far away at the starting point and hence have a very weak effect of the starting force. The effect, however, is still as predicted.

3.6.3 Effect of In-Plane Finger Length

Changing the finger length on the mask pattern has the same effect as changing the etch depth in standard X-Y comb drives. As shown in Figure 3.12, both the starting force and the maximum force double when the finger length is doubled. The range of the comb drive is independent of finger length.
3.6.4 Effect of Voltage

Figure 3.13 shows that at any displacement, the force is linear with respect to the square of the voltage as in a standard comb drive.
3.6.5 Effect of Vertical Separation between Levels

Processing variables control the vertical gap between shadow masked levels to a large extent. As discussed earlier, the vertical gap is minimum when the release etch preceding the shadow etch is perfectly isotropic. The gap also depends on whether an extension etch is performed on the beams before they are released. Considering the case where there is no extension etch, half the etch would presumably scoop out the
silicon inside the beam itself. In this case the vertical gap would ideally be only half the width of the released beam since the release etch proceeds from both sides of the beam. The silicon scooped out from inside the beam creates an oxide overhang. This concept is illustrated in Figure 3.14.

![Figure 3.14 Smallest Possible Vertical Gap](image)

The effect of vertical gap is to reduce starting force. This phenomenon is shown in Figure 3.15. RIE 1 is 50 µm, RIE 2 is 60 µm, finger gap is 2.5 µm and finger length is 30 µm. F vs. z curves for 1 µm and 5 µm vertical gaps are plotted. Only the initial part of the plot is shown to illustrate the change in starting force.
Given the deeply detrimental effects of this gap, there is an interesting tangent that the argument takes at this point. We go back to the comparison between total overlap and partial overlap Z actuators. It is interesting to note that the same shadow masked, non-overlapping actuator can be converted to a total overlap actuator simply by changing the biasing scheme. If both levels of the fixed fingers are grounded in spite of the isolation segment, the movable finger and the substrate can be grounded and this would immediately resemble a total overlap actuator as illustrated in Figure 3.16.
This change in bias has no apparent significance except that a total overlap actuator produces larger starting force than a non-overlapping actuator. Figure 3.17 shows the effect of initial bias on the Force – Displacement profile. While the total overlap actuator starts at a higher force and drops down fast, the non-overlapping actuator starts at a lower value and then ramps up to the constant maximum force. If the bias on the lower level fixed fingers can be externally ramped down from +V to ground while the movable finger travels through the vertical gap, we might be able to use the
positive aspects of both systems of actuation and travel from a high starting force to a constant force.

Figure 3.17 Effect of Initial Bias on Starting Force

Unfortunately this biasing scheme is not as simple as it seems. If the whole process is to be implemented with a single mask on a regular wafer with front side processing, the lower level of the fixed fingers has to be released from the substrate because it has to remain electrically isolated from the grounded substrate. The fixed fingers will be connected to a bonding pad that looks like a honeycomb. If the line widths on the
bonding pad are equal to or less than the fixed finger widths, then the bonding pads will release and there will be no mechanical anchor for the fixed fingers. If the line widths on the bonding pad honeycomb are higher then there is the risk of shorting out the two levels because the neck between the levels will not be oxidized through. The bonding pad will essentially have to remain electrically isolated but mechanical connected to the substrate. This is possible if there is an oxide layer at that location if we use an SOI wafer. Wafer bonding and backside etch techniques can also be used to get around this problem but both methods need multiple masks and additional alignment. SOI wafers with a thin oxide layer at the first neck location also alleviate the problems with vertical gap to a great extent.

The most obvious solution to the starting force issue is to use a three level process that combines the two level oxidation based process with shadow masking. Once the thin fingers are oxidized and the floor oxide is cleared, a short extension etch of 5 µm or greater is performed before release. After the extension etch, the sidewall is passivated, the floor is cleared and the thin beams are released leaving a short neck on the wider beams. Then the third level shadow extension etch is performed as usual. The extension etch RIE 2 is chosen to be 5 µm or greater because the vertical gap during release is usually in that range. The RIE 2 segment needs to guide the actuator through until the lower level overlaps the top level, without a considerable drop in force.

Figure 3.18 shows comparison plots of two level and three level actuators. RIE 1 is 50 µm, the shadow etch is 60 µm, finger gap is 2.5 µm, finger length is 30 µm and the vertical gap is 3 µm. All these parameters are exactly the same for both the two level
and three level actuators except that the three level actuator also includes a 5 µm RIE 2.

![Three Level Comb Fingers RIE, Extension, Release, RIE](image)

Figure 3.18 Two Level and Three Level Z Actuator Comparison

The force for the 3 level actuator starts at $8.56 \times 10^{-11}$ N and stabilizes at $9.4 \times 10^{-11}$ N. The force for the 2 level actuator starts at $1.99 \times 10^{-11}$ N and stabilizes at the same value as the 3 level actuator. This huge advantage in starting force makes the 3 level shadow masking process a prime candidate for out-of-plane actuation.
While three level shadow masking is certainly the holy grail for Z actuators, there are a few electrical and mechanical issues with this process. Let us examine three important issues associated with this process:

1. If the vertical gap is too large, then the RIE 2 extension will not help much. It will still help with the starting force because it will work as a total overlap comb drive but the force will fall off very fast before the lower level fingers can make it through the gap. Fortunately, we are concerned about the vertical gap only at the finger locations, which are confined to narrow spaces. Narrow spaces are loaded more during the RIE etch steps and vertical gaps would be smaller here. If there is a spring in an open area for instance, the loading effect can be large enough to create a release gap of 20 to 30 µm below the spring before the smaller gaps in the device are released.

2. If the process were to remain both single mask, the electrical ground for the lower level of the movable structures has to go through the spring suspension. This would mean that the spring is a composite mechanical beam with very thick oxide on the top level that was formed when the thin fingers were oxidized through.

3. All actuator support structures would be the same line width as the thin fingers so that they are eventually released in the lower level. We would then have a two level moving structure where each level is released independently and the two levels do not have a mechanical connection. Possibly the only way around this problem is to make all thin finger support structures the same width as the fixed fingers so that all levels remain mechanically connected at the isolation
neck. Final lower level release has to be provided using a separate mask with backside etching. The backside alignment will be non-critical and can hence be done crudely be hand.

The two level shadow masking process, on the other hand, is easier to implement. There is one less extension etch, sidewall passivation and floor clear step. The springs are still composite because the top level is oxidized through. An oxide etchback can be used to remove the entire top level oxide and this would solve the issue with composite springs and also etch away all top level moving structures. There will also be no independently released moving levels without a rigid mechanical connection, thus eliminating the need for a second mask and backside release.

### 3.7 Vertical Motion Approximation

The angular twisting motion of the actuator approximates the vertical motion created by the Z comb drive. It remains to be shown that for small angles, there is not much difference between the rotation and a vertical motion. Figure 3.19 shows the unwanted horizontal displacement that arises due to the rotation at the torsion spring. The horizontal motion is tabulated as a function of angle of twist in Table 3.1. It can be seen that the horizontal motion is noticeable only at 20° tilt. Even at this tilt, the horizontal motion is only 7.5 µm compared to the vertical displacement of 42.8 µm. As long as the in-plane finger overlap is greater than 7.5 µm, the comb drive will still function effectively. Adequate care must be taken that there is enough space at the finger ends so that the horizontal movement does not cause any collision with neighboring structures.
Figure 3.19  Horizontal Displacement in Z Actuator due to Torsion Spring

Table 3.1  Unintended Horizontal Displacement

<table>
<thead>
<tr>
<th>Angle of Twist (Degrees)</th>
<th>Lever Arm (µm)</th>
<th>Vertical Z Displacement (µm)</th>
<th>Horizontal Displacement (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>125</td>
<td>10.9</td>
<td>0.5</td>
</tr>
<tr>
<td>10</td>
<td>125</td>
<td>21.7</td>
<td>1.9</td>
</tr>
<tr>
<td>15</td>
<td>125</td>
<td>32.4</td>
<td>4.3</td>
</tr>
<tr>
<td>20</td>
<td>125</td>
<td>42.8</td>
<td>7.5</td>
</tr>
</tbody>
</table>
3.8 Conclusions

It has been shown that if true out-of-plane actuation with large range, large force and constant force needs to be achieved then a non-total vertical overlap between the fixed and moving levels is required. The simple two level process that was shown to create total overlap Z comb drives in Chapter 2 had linear force fall-off and a range of motion approaching half the height difference between levels. The partial overlap and non-overlap Z comb drives double the range of motion and maintain the force constant through the entire range with the addition of a few processing steps.

Shadow masking was used as a way to replicate the largest width on a lower level. Device designs with non-overlapping and partially overlapping comb fingers were demonstrated. Both designs are vastly superior to total overlap drives that are created simply by the two level process alone. The two level process is first implemented to oxidize lines of smaller width. It is either followed immediately by a release and shadow masking step to create non-overlapping comb fingers, or it is followed by a short extension etch before the release and shadow masking to create partially overlapped comb fingers. The short extension serves as the initial overlap during the early stage of motion.

Figure 3.20 shows and a comparison between a total overlap Z drive and a partial overlap Z drive. The graphs are overlaid for a 2.5 µm finger spacing and a 10 µm height difference between levels. The higher range and constant force for the partial overlap comb drive are apparent from the graphs.
Vertical gap was explained and the effects of this gap on Z actuator designs were demonstrated. Vertical gap reduces the starting force. Several methods were discussed, including biasing schemes and process modifications, that can compensate for this gap by increasing the starting force.

Finally the pros and cons of the two level and three level shadow masking process were discussed. Two level shadow masking has fewer process steps and is easier to implement. The starting force in the comb drive is however quite low because of the absence of the initial overlap segment. Once the lower level comb finger enters the upper level fixed finger system, the force reaches its maximum constant value. The
three level shadow masking process, though more complex, is the closest approximation to a conventional comb drive.

We have demonstrated the concepts behind a nearly ideal Z actuation system. The partial overlap and non-overlap designs are similar in nature and will be used to design a moving micromirror for optical applications in the following chapters. Since device footprint is always a concern, we need the largest possible force with the smallest number of actuators. The largest range of motion with the shortest possible etch depth also gives the lowest possible moving mass.
4.1 Introduction

The subject of this chapter is the design and fabrication of MEMS micromirrors with a given list of performance specifications. The micromirrors could be used for various applications including adaptive optics, display devices, fiber optic switching and free space communications. These applications usually require an array of moving micromirrors. The designs presented here are for a single micromirror device. While the designs are potentially scalable, issues involved with arrays of mirrors are not explored in this thesis.

The micromirror is mounted on a torsional spring and the mirror twists on either side of the torsional axis of that spring by means of Z actuator banks located on each side. A preliminary schematic is shown in Figure 4.1. The linear out-of-plane movement of the actuator is approximated by the angular twisting movement of the torsion spring. The design specifications include constraints on the response time of the mirror, the twisting frequency and the maximum angular displacement. These in turn impose constraints on the mechanical characteristics such as device geometry and material composition and electrical characteristics such as actuator geometry, number of actuators and voltage. There are additional constraints on process parameters and mask layout based on all these factors. This chapter first lays out the performance specifications provided and then describes detailed mechanical, electrical and process
design issues in relation to the performance specifications. Mechanical and electrical design results are used to arrive at device geometry and process parameters, while known constraints in geometry and processing are in turn applied to restrict the electromechanical design. Based on these results, multiple process flows are proposed together with the advantages and drawbacks of each method.

Figure 4.1  Mirror Mounted on Z actuator with Torsional Spring: 3-D Schematic
Note that the comb banks are multilevel structures in Figure 4.1. They have comb fingers with equal and opposite in-plane forces in X and Y, so that movement is in Z alone. The torsion spring suspends the mirror and the Z comb actuators and provides the electrical path to the moving fingers. The fixed fingers on either side are connected to separate bonding pads elsewhere on the chip. The actuators can move up or down depending on which side is actuated. Total overlap Z actuators are simple to fabricate but will not have sufficient performance characteristics for the micromirror device. Only partial overlap and non-overlapping Z actuator designs are examined in the chapter. These designs give the required constant force profile over the entire range of motion. Their larger range for a given etch depth allows lower mass for higher resonance frequency.

4.2 Design Considerations

Bulk micromachining is used for making the micromirror device because it produces a monolithic, single crystal structure in silicon with very high strength and reliability. No sliding parts such as hinges are used in the design. All movement is by flexure, thus reducing friction and wear. High aspect ratio structures have the added advantage of stiff springs and large resonance frequencies with reduced cross axis response. High frequency, large displacement torsional springs impose a strict requirement on the material strength and single crystal silicon is the preferred solution.

Single mask processing is attempted to the extent possible, so that there is no need for patterning across large steps. If multiple masks are used, it is useful to ensure to the
extent possible that alignment needs are not critical. Single mask processing improves yield significantly.

The process should be robust enough so as to produce devices of repeatable consistency across a large array. In other words, both the design and the process should be scalable. The mirror would ideally be formed in the same processing steps as the actuator, so that bonding steps are avoided. Finally, it would be interesting to have a design and process that can be scaled from a single axis to a two axis mirror.

4.3 Device Specifications

The design specifications provided for this device are as follows:

1. 5 to 20 degrees tilt on either side of the torsional spring
2. 5 kHz - 50 kHz resonance frequency
3. 20 $\mu$s – 50 $\mu$s response time
4. 50 to 200 $\mu$m square mirror

4.4 Parameter Dependence and Trade-Offs

Torsion spring equations describing dynamics and stress for a rectangular cross section are available in literature [1-3]. The mirror tilt is controlled by the stiffness of the torsion spring and the applied torque. $\tau = k_\theta \theta$, where $\tau$ is the torque in Nm, $k_\theta$ is the torsional stiffness in Nm/rad and $\theta$ is the angle of twist in radian.
Soft springs are required for large tilt angles such as those specified here. The torque is a function of the actuator design parameters such as comb finger length, comb finger gap, amount of oxide present, number of comb fingers, the driving voltage and the separation between the mirror and the actuator. The torque increases linearly with increasing finger length, increasing finger count, increasing voltage squared and decreasing finger gap. It increases weakly with the amount of oxide on the actuator. The separation between the spring and the actuator bank is the torque arm. A larger torque arm implies a requirement of lower actuation force but larger Z displacement for the same tilt angle.

The resonance frequency of the device is given by:

$$\omega = \sqrt{\frac{k_g}{I_z}} \quad \omega = 2\pi f$$

where $\omega$ is the resonance frequency in rad/s, $f$ is the resonance frequency in Hz and $I_z$ is the polar mass moment of inertia. The large resonance frequency requirement means that the spring has to be stiff or the polar mass moment has to be small. Stiffer springs are in direct opposition to the soft spring requirement for large tilt angles. The design will have to balance both these requirements.

The polar mass moment of inertia for a rectangular cross section is given by:

$$I_z = \frac{m}{12} \left( L_s^2 + b_s^2 \right)$$

where $m$ is the effective mass of the moving structure, $L_s$ is the length of the spring and $b_s$ is the height of the spring into the wafer. The mass needs to be adjusted to
account for the total effective mass of the comb fingers and support structures in addition to the mirror and spring. A reduced effective mass will mean higher resonance frequency.

For a fixed-fixed torsion beam loaded at the center, the torsional stiffness is given by

\[
k_{\theta} = \frac{4G}{L_s} \left( \frac{a_s^3 b_s}{3} - \frac{3.36a_s^4}{16} \left( 1 - \frac{a_s^4}{12b_s^4} \right) \right)
\]

where \( G \) is the shear modulus of the material and \( a_s \) is the width of the spring. The stiffness thus increases with increasing etch depth and decreasing spring length. It increases very strongly with the width of the spring. For high aspect ratio torsion bars, we have \( a_s \ll b_s \) and the expression for stiffness reduces to:

\[
k_{\theta} \approx \frac{4G}{3} \left( \frac{a_s^3 b_s}{L_s} \right)
\]

The mirror size influences the performance in two ways. Larger mirrors mean a larger moving mass. In addition, the actuators need to be farther away from the spring for larger mirrors. This increases the torque arm, thus requiring larger displacement but reduced force for the same torsion angle.

The relation between the resonance frequency and the response time depends on the damping coefficient in addition to geometrical parameters. A first order analysis can be used to arrive at the fastest possible response time. As shown in Figure 4.2, the
time taken to travel from the equilibrium position to the maximum displacement is one-fourth the time period. The fastest possible response time is hence given by

\[ T_{\text{response}} > \frac{1}{4f}, \text{ or } \]
\[ T_{\text{response}} > \frac{\pi}{2\omega} \]

Once the mirror reaches the maximum tilt in this time, the additional time required for stabilization depends on the damping.

![Diagram of Fastest Response Time](image)

Figure 4.2 Fastest Response Time Diagram

The design has to achieve a small stiffness for large angular displacements at reasonable voltages and a corresponding mass and geometry and possibly conflicting stiffness for large resonance frequencies. Conflicting requirements are solved by controlling geometrical parameters suitably.
4.5 Electromechanical Design

4.5.1 Frequency and Displacement Analysis

The resonance frequency is calculated for several spring dimensions. For the purpose of this analysis, the mass is kept constant based on a mirror size of 100 μm and an actuator bank of 50 comb fingers. Once we have a range of values for frequency, we can then iterate the mirror and comb drive parameters.

Table 4.1 shows the frequency calculation for spring widths varying between 1 μm and 3 μm and a spring etch depth between 10 μm and 50 μm.

<table>
<thead>
<tr>
<th>a (μm)</th>
<th>b (μm)</th>
<th>L (μm)</th>
<th>kθ (Nm/rad)</th>
<th>m (kg)</th>
<th>Iz (kg.m²)</th>
<th>ω sqrt(kθ/Iz)</th>
<th>f₁ (kHz)</th>
<th>Fastest Response Time (μs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>10</td>
<td>100</td>
<td>6.9E-09</td>
<td>1.6E-09</td>
<td>1.3E-18</td>
<td>71432</td>
<td>11</td>
<td>22</td>
</tr>
<tr>
<td>1.5</td>
<td>25</td>
<td>100</td>
<td>1.8E-08</td>
<td>1.6E-09</td>
<td>1.4E-18</td>
<td>112317</td>
<td>18</td>
<td>14</td>
</tr>
<tr>
<td>2.27</td>
<td>25</td>
<td>100</td>
<td>6.0E-08</td>
<td>1.6E-09</td>
<td>1.4E-18</td>
<td>205001</td>
<td>33</td>
<td>8</td>
</tr>
<tr>
<td>1</td>
<td>50</td>
<td>100</td>
<td>3.6E-08</td>
<td>1.6E-09</td>
<td>1.7E-18</td>
<td>147387</td>
<td>23</td>
<td>11</td>
</tr>
<tr>
<td>1.5</td>
<td>50</td>
<td>100</td>
<td>1.2E-07</td>
<td>1.6E-09</td>
<td>1.7E-18</td>
<td>269901</td>
<td>43</td>
<td>6</td>
</tr>
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<td>2.27</td>
<td>50</td>
<td>100</td>
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<td>1.6E-09</td>
<td>1.7E-18</td>
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<tr>
<td>3</td>
<td>50</td>
<td>100</td>
<td>9.5E-07</td>
<td>1.6E-09</td>
<td>1.7E-18</td>
<td>756007</td>
<td>120</td>
<td>2</td>
</tr>
</tbody>
</table>
The first two entries in Table 4.1 have an etch depth of 10 μm. This implies that the spring is made in a separate masking step since the actuator depth needs to be considerably higher for large tilt. The width is varied between 1μm and 2μm and the corresponding frequency ranges from 11 kHz to 31 kHz.

For the 25 μm etch depth on the spring, we vary the spring width between 1 μm and 2.27 μm. This choice of etch depth could mean that the top level of the spring is oxidized through and then etched back, so that the spring is present only on a 25 μm lower level. It could also mean that the actuator is 12.5 μm tall on each level giving a Z displacement of about 12 μm with the spring extending across both levels. The 1 μm width is shown here for the sake of comparison with the shorter spring case. A 1 μm spring on the top level would appear as a 2.27 μm wide spring on the bottom level if the top level is oxidized through, while the 1.5 μm width is an indication of an approximate average width if a two level spring is used. The corresponding frequency ranges from 18 kHz to 60 kHz.

For a Z displacement of 25 μm in either direction, the total actuator depth across both levels is 50 μm. The width variations in this case show a series of average width values corresponding to a wide choice of starting widths on the top level of the spring. Given the large etch depth, we would have to choose a fairly wide spring to survive the long etch. A 2 μm wide spring, for example, might be approximately 3 μm wide when averaged across both levels, depending on how much of the spring is oxidized through before shadowing. The frequency range for this case is 23 kHz to 120 kHz.

It can be seen that the spring width has to be at least around 2 μm to approach a 50 kHz resonance frequency, while for frequencies in the lower range, we will either need
a two mask process or low etch depths or both. Spring height and length have smaller effects on the stiffness compared to the spring width.

The next step is to find out how much displacement these springs can produce, or rather, how much voltage is required to produce a certain angular displacement. For all the stiffness values on the table, we compute the voltage required to tilt the mirror 5°, 10° and 20°. The voltage is computed to maintain the number of fingers at approximately 50. Given the size of the mirror, this is a reasonable starting assumption because 50 fingers would take up approximately as much space as the mirror size plus the spring length and the supports.

Table 4.2 lists the voltage calculations for different spring sizes and torsion angles. A torque arm of 125 μm is used in the calculations. This value is half the mirror size plus an estimated distance between edge of the mirror and the center of the comb finger bank. An interesting feature of our design is that the Z actuator is also an in-plane actuator because it also looks like a regular comb drive. As shown in Figure 4.3, the comb finger bank will need to contain equal and opposite finger pairs to create in-plane equilibrium while allowing only Z motion. The means that the 80 fingers assumed in this calculation will be stacked in pairs. This kind of stacking increases the distance between the spring and the actuator bank because the comb fingers are effectively farther away from the mirror when stacked. Electrostatic design, as calculated in previous chapters, shows that the force on a typical partial overlap Z comb drive is $9.37 \times 10^{-11}$ N per finger per Volt once the force becomes constant, when the comb finger gap is 2.5 μm, the finger overlap is 30 μm and the two levels are each about 25 μm tall. This typical value of force is used in the table to arrive at the required voltages.
Table 4.2  Voltage and Displacement vs. Stiffness

<table>
<thead>
<tr>
<th>Stiffness (Nm/rad)</th>
<th>θ (Deg)</th>
<th>Force Arm (l) (μm)</th>
<th>Displacement z=lθ (μm)</th>
<th>Force (N)</th>
<th>Voltage (Volts)</th>
<th>Fingers n=kφ/T/V²</th>
</tr>
</thead>
<tbody>
<tr>
<td>6.9E-09</td>
<td>5</td>
<td>125</td>
<td>11</td>
<td>9.37E-11</td>
<td>36</td>
<td>79</td>
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<td>6.9E-09</td>
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<td>125</td>
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<td>6.9E-09</td>
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<td>125</td>
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<td>5.1E-08</td>
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<td>125</td>
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<td>9.37E-11</td>
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<tr>
<td>5.1E-08</td>
<td>20</td>
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<td>9.37E-11</td>
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<td>80</td>
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</table>
For a $10^\circ$ tilt on either side of the mirror, we compare the voltages required for different values of stiffness. It is apparent from Table 4.2 that a two mask process, shown by the first two values of stiffness, would be ideal in terms of operating voltage. The mirror would tilt $\pm 10^\circ$ for either 51 V or 139 V, depending on spring width. The actuators will still have to be about 25 $\mu$m tall on each level to enable the 22 $\mu$m Z displacement required for this angle and lever arm.
Figure 4.3 Canceling In-Plane Forces in Z Drives

Figure 4.4 Voltage Across Thin Oxide: SCREAM Isolation with Metal
Single mask devices are easier to fabricate. For the single mask case, we will either have a two level spring or a lower level spring with the top level oxidized through and etched back. The corresponding operating voltage for a lower-level-only spring that is 25 µm tall is 273 V. A two level spring that is 12.5 µm tall on each level requires 150 V. If each level is 25 micron tall, then a narrow spring requires 212 V while a wide spring requires between 350 V and 600 V depending on the width. Given that the Z displacement has to be 22 µm, we will have to have about 25 µm etch depth per level resulting in a total 50 µm depth on the spring. The only two possibilities here are hence the 25 µm lower level only spring and the 50 µm tall two level spring. The spring should be as narrow as possible for low stiffness, but wide enough to survive the first 25 µm deep RIE step. Whatever the first level width of the spring, it will be
wider after thermal oxidation and the second 25 μm deep RIE step will not pose any problems.

The standard SCREAM process uses metal as the conducting material and the core substrate silicon is usually grounded. This places a limit on the largest operating voltage such that the electrical integrity of the thin sidewall oxide between the metal and the silicon core is maintained. Here we use highly doped substrate silicon as the conducting material with appropriate oxide segments for vertical isolation. The largest voltage is determined here by the thickness of the vertical isolation. Figure 4.4 and Figure 4.5 illustrate both schemes. Thick vertical segments allow large operating voltages while thinner segments minimize the vertical gap between levels, thus aiding initial actuator motion.

The calculations use very conservative estimates and it is possible that the displacement and frequency performance can be achieved even at lower voltages. The devices could also have a larger number of comb fingers and multiple stacks to help increase the force. In reality, the mask layout has several design variants on comb finger, spring and mirror geometry so that the entire design space is covered. Once fabricated, a small set of these variants will yield optimum performance.

One particular design variant on the mask is a 200 μm mirror with 88 comb fingers on each side. It is suspended on a torsion spring that is 1.5 μm wide, 50 μm tall and 100 μm long. This device is designed to move 5 degrees on each side with 140 V and 10 degrees with 200 V.
Additionally, the mirror, torsion spring, supports and comb finger banks were modeled in ANSYS as shown in Figure 4.6. The geometric shapes were created on a 1:1 scale and meshed using 10 node tetrahedral elements with rotations in all directions. ANSYS was used to model both torsional and in-plane modes. The numerical results are compared to analytical calculations.

Table 4.3 shows the comparison between analytical and ANSYS values for the torsional frequency. The frequency is denoted by $f_1$ because it is the frequency of the first mode. Figure 4.7 is a plot of these values to show that there is a close match. The difference arises because the polar mass moment of inertia is approximated in the analytical calculations. All the mass of the structure is assumed to be concentrated at the spring but the mass is doubled to account for the additional inertia of the extremities. ANSYS better accounts for the distributed mass. While the voids in the
honeycomb structures are not modeled in ANSYS so as to reduce the complexity, the material density is appropriately lowered to account for the reduced mass due to the voids.

Figure 4.7 Analytical and ANSYS Values of Torsional Frequency
<table>
<thead>
<tr>
<th>$a$ (µm)</th>
<th>$b$ (µm)</th>
<th>$L$ (µm)</th>
<th>$f_i$ (Torsion) (kHz) $^{\text{Analytical}}$</th>
<th>$f_i$ (kHz) $^{\text{ANSYS}}$</th>
</tr>
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<tbody>
<tr>
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<tr>
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<td>50</td>
<td>100</td>
<td>120</td>
<td>125</td>
</tr>
</tbody>
</table>

4.5.2 In-Plane Frequency Analysis

It is important that the first two modes of vibration of the device are properly decoupled so that we do not see unintended modes of vibrations when the device is operated at the torsional resonance frequency. The first mode is the torsional mode and the second mode is the mode of in-plane twisting. The second mode shape is shown in the ANSYS simulation in Figure 4.8. It has been shown that the addition of a wide bar close to the center of the torsion spring separates the frequencies of the torsional and in-plane modes [3]. An example of a bar that has a larger width than the spring is shown in Figure 4.9. The size of this bar can be tuned to control the frequency separation.
Figure 4.8  In-Plane Twisting: Second Mode of Vibration

Figure 4.9  Wider Bar on Torsion Spring Separates Frequencies
In our case, the size of the mirror is comparable to the length of the torsion spring and the mirror itself acts as a very wide and very long bar, thus automatically separating the modal frequencies. The separation thus achieved is far superior to that achieved by using a bar because the mirror is naturally much larger as shown in Figure in 4.10.

![Figure 4.10](image)

**Figure 4.10**  Mirror as Wide Bar on Torsion Spring for Frequency Separation

The stiffness of the in-plane mode is denoted by $k_\phi$ and is given by the following expression:

$$k_\phi = \frac{2E\alpha^3b}{3L_eL_T}\left(1 + \frac{3L_e}{2L_T}\right)$$
where $L_c$ is the torque arm, $L_T$ is the length of one side of the torsion spring, $L^*$ is the length of the frequency separation bar, or, in this case, half the length of the mirror. $\varphi$ is the in-plane angle of twist.

Table 4.4 shows calculations comparing the torsional and in-plane frequencies. The in-plane frequencies with and without the mirror are shown to demonstrate the important role the mirror plays in frequency separation. The table shows analytical results. ANSYS simulations were used to generate the first five modes of the device. The simulations showed larger in-plane frequency than the analytical results, thus showing better frequency separation.

Table 4.4 Frequency Separation between Modes caused by the Mirror

<table>
<thead>
<tr>
<th>$a$ ($\mu$m)</th>
<th>$b$ ($\mu$m)</th>
<th>$L$ ($\mu$m)</th>
<th>$f_1$ (Torsion) (kHz)</th>
<th>$f_2$ (in-plane) (kHz)</th>
<th>$f_3$ (in-plane) (kHz)</th>
</tr>
</thead>
<tbody>
<tr>
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<td></td>
<td></td>
<td>With Mirror</td>
<td>With Mirror</td>
<td>No Mirror</td>
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<td>100</td>
<td>120</td>
<td>6822</td>
<td>1365</td>
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</table>

Figure 4.11 shows a plot of the three frequency values so that the modal separation and the effect of the mirror are clearly seen.
4.5.3 Stress Analysis

Analytical calculations and numerical calculations with ANSYS were used to model the maximum stress on the torsion spring. The largest von Mises stress in the spring cannot exceed the fracture stress of silicon at ±10 degrees tilt. The fracture stress for single crystal silicon has been reported to be about 3.4 GPa [5-10]. A Young’s modulus of 125 GPa and a Poisson’s ratio of 0.28 are used in the calculations.

The maximum shear stress in torsion is given by
\[ \tau_{\text{max}} = \frac{3T}{a^2b} , \]

where \( \tau_{\text{max}} \) is the maximum shear stress in the torsion spring. \( T \) is Torque on the spring or half the torque applied by the comb finger bank because the applied torque is felt in equal proportion by either half of the fixed-fixed spring.

Figure 4.12 shows an ANSYS simulation for a 2 \( \mu \text{m} \) wide 10 \( \mu \text{m} \) tall torsion spring with tilt of 5 degrees. The tilt has been exaggerated for clarity. The maximum stress of 0.36 GPa can be seen in the closer view of the spring in Figure 4.13.
Stresses are calculated using both the analytical expression and ANSYS for the entire range of useful stiffness values of the spring. The results are tabulated in Table 4.5. The analytical and ANSYS values agree well as shown by the graph in Figure 4.14 because unlike in the case with the frequency analysis, there are no differences in quantities such as the polar moment of inertia based on distributed mass. Different comb finger and support structure configurations translate only to different voltage requirements for the same tilt on the spring. The stress on the spring depends only on the spring geometry and the tilt angle.
### Table 4.5 Maximum Stress on Torsion Spring: Analytical and Numerical

<table>
<thead>
<tr>
<th>$a$ ($\mu$m)</th>
<th>$b$ ($\mu$m)</th>
<th>Stiffness (Nm/rad)</th>
<th>$\theta$ (Deg)</th>
<th>Voltage $V$ (Volts)</th>
<th>Shear Stress Analytical (GPa)</th>
<th>Shear Stress ANSYS (GPa)</th>
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<td>20</td>
<td>840</td>
<td>2.21</td>
<td>2.16</td>
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For a torsional spring ending straight at the support, there is a stress concentration at the corner as seen by the dark spot at the top left corner of Figure 4.15. This stress concentration is alleviated by adding brackets at the spring ends. Figure 4.16 shows a more distributed stress in the presence of the bracket. The bracket is small enough and rigid enough not to alter the dynamic characteristics of the spring appreciably.
Figure 4.15  Stress Concentration on Torsion Spring near Support

Figure 4.16  Stress Better Distributed with Bracket
4.5.4 Spring End Design for Compressive Stress

The device experiences long oxidation times during the process flow because thin beams have to be consumed to create the multiple levels required for Z actuation. Thermal oxidation causes a compressive stress that creates a longitudinal push on the torsion springs towards the mirror. If the spring is released or if it is very compliant during oxidation, it causes it to buckle. Figure 4.17 shows an ANSYS simulation of this buckling effect. Electron micrographs of this effect on the actual device will be shown along with process results.

![Figure 4.17 Buckling of Released Spring due to Compressive Stress](image)

To prevent buckling, we modify the spring ends to include a butterfly shaped bracket. The bracket has to be compliant enough to take all the deformation due to thermal...
oxidation and still not appreciably affect the frequency and displacement characteristics of the spring. The bracket design shown in Figure 4.18 satisfies these conditions. ANSYS was used to simulate the bending of this bracket due to oxidation induced deformation. Figure 4.19 and Figure 4.20 show the bracket deforming to take the stress in the spring so that the spring remains straight. The displacements have been exaggerated for clarity.

Figure 4.18 Spring End Design to Prevent Buckling
Figure 4.19  “Butterfly” Bracket for Stress Relief: Before Oxidation

Figure 4.20  “Butterfly” Bracket for Stress Relief: After Oxidation.  Spring Straight
4.6 Process Design

4.6.1 Two Mask Front Side Process Flow

4.6.1.1 Motivation

We have seen that the actuator banks need to be about 50 μm tall in total across both levels to achieve the 25 μm vertical displacement required for 10 degrees tilt. We would ideally need the spring to be of smaller height so that we have independent control of spring stiffness and actuation force. A reduced mirror height would translate to a lower moving mass. A two mask process would be required to achieve this flexibility. Additionally, if all processing is to be done from the front side, thus eliminating the need for backside alignment, the mirror cannot be a solid block. There will need to be honeycomb etch vias in the mirror block. These vias need to be sized such that the holes fill in during a subsequent thermal oxidation step in the process. The mirror would finally need to be polished to get a smooth surface. Alternatively, a mirror would be fabricated on a separate wafer and bonded to the device.

While bonding of full wafers and even individual dies to each other is well known, there has not been any report, to our knowledge, on bonding to released MEMS structures. The mask contains test structures to test the bonding process. A process for oxygen-plasma activated silicon direct bonding has been developed in the research group by Dr. Masaru Rao. It has been tested on unprocessed wafers and has been shown to yield bond strengths well within the range needed for micromechanical applications. There is concern, however, that the surface roughness after processing may prove to be too large for good direct bonding. Other alternatives such as using
intermediate bonding layers such as spin-on-glass, BCB, metal bump bonding, etc are possibilities.

4.6.1.2 Mask 1 Process Flow

The process flow for the first mask in the two mask process is shown in Figure 4.21. Constraints on device geometry and process parameters will be deduced from the process flow. The following symbols are used in the process flow diagram to arrive at the constraints:

- \( w \): Thickness of initial mask oxide
- \( x \): Width of movable fingers
- \( y \): Width of fixed fingers \((x < y)\)
- \( g \): Initial gap between fixed and movable fingers
- \( RIE1, RIE2, RIE3 \): Height of first, second and third levels. The second level is optional and is the short overlap segment required for a true partial overlap comb drive.

Any range of values shown along with the process steps corresponds to the range in movable finger width \( x = 0.5 \ldots 1 \) \( \mu m \) and a corresponding fixed finger width \( y = 2 \ldots 2.5 \) \( \mu m \).
1. Thermal Oxide, Thickness = *w*

![Mask 1 Diagram]

2. Pattern Oxide

![Pattern Oxide Diagram]

3. Silicon deep RIE, Etch Depth = RIE1

![Silicon deep RIE Diagram]

Figure 4.21 Two Mask Front Side Process Flow: Mask 1
4. Oxidize Thin Fingers Through
Oxidation Time: To grow 1.135x oxide (1100 C, Wet)

5. Floor Clear
6. Overlap Extension Etch (Etch Depth = RIE2)

7. Sidewall Passivation 0.1-0.2 μm Thermal Oxide

Notes:
Dimension changes < 100nm: ignored.
8. Floor Clear

9. Timed Release
   Release thin beams completely
   Partial Release of Wide Beams - Short neck remains
10. Thermal Oxidation

Oxidize 0.5 μm neck through

Oxidation Time: $0.6 \times 1.135 = 0.68 \, \mu\text{m oxide}$

Slightly over-oxidize to consume 0.3 μm Si.

11. Floor Clear: Etch 0.68 μm oxide

10(a) Optional Dilute BHF dip: Remove Overhang
12. Extension Etch RIE3

13. Sidewall Passivation
0.1-0.2 mic thermal oxide
Figure 4.21 (Continued)

14. Floor Clear

15. Extension Etch & Release

Extension etch > Range of motion
RELEASE BEAMS OF WIDTH 2.27x
DO NOT RELEASE WIDER BEAMS
4.6.1.3 Process Description

Steps 1 through 8 in Figure 4.21 are essentially the same as the two/three level process flow as described in earlier chapters. The silicon finger reduces in width as we move through the process flow, while the total finger width including sidewall oxide increases, thus reducing the gap. The mask oxide on the top is depleted with every floor clear step. In reality, there needs to be an additional oxide over-etch at every floor clear step because the oxide etch RIE process etches the open areas much faster than the smaller and deeper gaps. This means that depending on the amount of oxide over-etch needed, mask oxide depletion will be faster than shown in the process flow.

Step 9 is a timed release step where thin fingers are completely released and wider fingers have a silicon neck. The etch via size is very important during the release step as structures to be released at similar rates need to be loaded similarly. For example, a structure that should not be released cannot be placed in an open area even if it is moderately wider than a released structure.

The neck is oxidized through to form the electrical isolation in Step 10. Step 12 shows the shadow extension etch. With the short overlap segment created in Step 6, we have a true three level structure that forms the partial overlap comb drive. The overlap segment \( RIE \ 2 \) is optional. It serves to increase the starting force as shown in previous chapters. Release of the lower level completes the 3 level Z actuator.
4.6.1.4 Electrical Isolation

The two levels of the fixed finger are isolated by the vertical oxide segment, while the two levels of the thin finger are connected through wider lines on the mirror. The lines on the mirror are similar to the large silicon structure shown on the left end of Step 15 in Figure 4.21 because the mirror is drawn as a large block in this mask. The spring and mirror honeycombs are fabricated in the second mask.

The electrical isolation scheme is shown in Figure 4.22.

In Figure 4.22, the large bonding pad has electrically connected levels. It is grounded through the substrate and also mechanically attached to the substrate. The fixed comb fingers have electrically isolated levels. The top level is biased and the bottom level is
grounded through the substrate. The thin comb fingers have silicon on the lower level only. Both levels are released and the lower level is grounded through the mirror structure. The honeycomb bonding pads are constructed exactly like the fixed fingers. They are used to provide electrical contact to the top level after etching off the mask oxide in the end. The mirror structure contains lines wider than the fixed fingers. Levels are not isolated and are eventually grounded through either level of the spring and finally through the substrate. Based on the Mask 1 process flow, there is no constraint on the line width of the mirror lines if they are exposed in a second mask. If they are only released in a second mask but exposed in the first mask, then the large line width constraint applies.

4.6.1.5 Process Constraints

Based on the process flow in Figure 4.21, we have the following conditions on geometry and process parameters:

1. SCREAM Mask Oxide Condition

The starting oxide thickness cannot be depleted before the final lower level release. Top level silicon will be exposed and etched if the oxide is depleted.

\[ w > 1.135x + 0.98 - (0.07 \ldots 0.23) \mu m \]

2. Finite Gap Condition

The finger gap should not completely close due to volume expansion by oxidation.

\[ g > 1.27x + 0.92 \mu m \]
3. Multilevel Condition

Fixed fingers should have upper level silicon and movable fingers should only have lower level silicon. There will be no Z actuation if this condition is not met.

\[ y - x > 0.18 \ldots 0.33 \mu m \]

4. Minimum Vertical Gap Optimization

The Silicon-Silicon vertical gap between the two levels should be minimized. Larger vertical gap reduces the starting force and the lower level comb finger would have to travel a longer distance before it enters the top level comb finger system. Vertical gap depends on the release parameters in Step 9 and also on device geometry. If the release is perfectly isotropic, the lateral etch rate will be equal to the vertical etch rate and the vertical gap will be a minimum. However, the parameters that make the release isotropic, such as low RF power, will increase loading and will etch small vias very slowly. A balance has to be achieved between loading and isotropic etching.

\[ y + 1.27x + 0.1 \mu m = \text{Minimum} \]

5. Minimum Horizontal Finger Gap Optimization

For maximum actuation force, the silicon cores in the fixed and movable comb fingers will have to be as close as possible.

\[ g - 0.135x - (0.33..0.38) \mu m = \text{Minimum} \]
Table 4.6 lists the final oxide thickness and final horizontal and vertical gaps after the Mask 1 process flow. Moving finger widths of 0.5 µm and 1 µm are considered. The corresponding fixed finger widths vary between 1 µm and 2.5 µm.

It can be seen that a starting oxide thickness of 2 µm is sufficient for the 0.5 µm fingers, while it falls short for the 1 µm fingers. 3 µm of mask oxide is hence a good working value both in terms of the process constraints and also in terms of the integrity of the pattern transfer from the photoresist to the oxide through the polysilicon.

The final oxide-oxide gap is the final physical in-plane gap between the fingers and determines the loading effect in the second level RIE etch. It is desirable to have this

![Table 4.6 Geometry Design Based on Process Constraints](image-url)

<table>
<thead>
<tr>
<th>x (µm)</th>
<th>y (µm)</th>
<th>Initial Mask Oxide (µm)</th>
<th>Final Mask Oxide (µm)</th>
<th>Initial Oxide Gap (g) (µm)</th>
<th>Horiz Si-Si Gap (µm)</th>
<th>Horiz Oxide Gap (µm)</th>
<th>Top Level Si Core Gap (µm)</th>
<th>Vertical Gap (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.5</td>
<td>1</td>
<td>3</td>
<td>1.5</td>
<td>3.5</td>
<td>3.1</td>
<td>1.9</td>
<td>0.17</td>
<td>1.7</td>
</tr>
<tr>
<td>0.5</td>
<td>2</td>
<td>3</td>
<td>1.5</td>
<td>2.5</td>
<td>2.1</td>
<td>0.9</td>
<td>1.17</td>
<td>2.7</td>
</tr>
<tr>
<td>0.5</td>
<td>2</td>
<td>2</td>
<td>0.5</td>
<td>3.5</td>
<td>3.1</td>
<td>1.9</td>
<td>1.17</td>
<td>2.7</td>
</tr>
<tr>
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<td>3</td>
<td>1.5</td>
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<td>3.4</td>
<td>1.17</td>
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<td>1.3</td>
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<td>0.3</td>
<td>1.2</td>
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</tr>
<tr>
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<td>2</td>
<td>-0.05</td>
<td>3.5</td>
<td>3.0</td>
<td>1.3</td>
<td>1.2</td>
<td>3.9</td>
</tr>
<tr>
<td>1</td>
<td>2.5</td>
<td>3</td>
<td>1.0</td>
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<td>4.5</td>
<td>2.8</td>
<td>1.2</td>
<td>3.9</td>
</tr>
</tbody>
</table>
gap to be at least around 2 µm, so that the finger gap can be carried through during the 50 µm etch. It can be seen from the table that the starting finger gap has to be at least 3.5 µm for the 0.5 µm fingers while a 5 µm gap is desirable for the 1 µm fingers. The horizontal Si-Si gap determines the actuation force and should be minimized to the extent possible, given the other constraints.

The vertical gap also has to be minimized and it ranges from 2.7 µm - 3.9 µm in the geometries of interest. The remaining thickness of the silicon core in the top level of the fingers should be at least 1 µm for mechanical and electrical integrity. It can be seen from the table that a good choice of moving and fixed finger widths would be either 0.5 µm and 2 µm or 1 µm and 2.5 µm respectively.

4.6.1.6 Process Variations

The Mask 1 process has 15 steps and is quite complex. There are a few simplifications that are possible in the process flow. As discussed earlier, the overlap segment is optional is the vertical gap between levels can be made small. The purpose of the overlap segment is to increase the starting force before the comb drive enters the upper level. Hence steps 6, 7 and 8 can be eliminated if Step 9 can be made close to isotropic. This reduces the process to 12 steps.

Additionally, if the overlap segment is eliminated, the two long thermal oxidation steps 4 and 10 can be combined into one because the oxidation for both the finger and the neck can be done after the first level is released. In this case, steps 4 and 5 are reduced to a short sidewall oxidation and a short floor clear step. The oxidation time in step 10 would be for the longer oxidation. For instance, a 0.5 µm neck and a 1 µm
thin finger in the device would mean that Step 10 oxidizes the 1 µm finger through
during which time the 0.5 µm neck is automatically oxidized through. However, an
unnecessarily long oxidation in Step 10, corresponding to comb fingers or necks that
are wider than required, will increase the Si-Si vertical gap and hence reduce the
starting force in the actuator. As seen in Step 15, the multilevel Si-Si gap for a neck
size of 0.5 µm is $y+1.27x+0.1$ µm.

4.6.1.7 Oxide Etch Issues

Once the mask oxide is grown in Step 1, the wafer is coated with photoresist. Then
the lithography is done and the pattern is transferred from the photoresist to the oxide
using CHF$_3$ RIE. Given the requirement for the thinnest possible fingers for the
shortest vertical gap between levels, the photoresist has to be chosen for high
resolution. High resolution generally implies that a very thin photoresist layer is used.
It is not possible to directly transfer a pattern on a thin resist to a high aspect ratio
oxide line on thick oxide because of the low selectivity of the CHF$_3$/O$_2$ etch or other
standard oxide etch recipes to photoresist.

A hard masking layer is needed to serve as an intermediate layer in the pattern
transfer. This masking layer is preferably not a metal so as to satisfy the cleanliness
requirements on most of the equipment in the clean room. Polysilicon is a good
choice for the intermediate layer. As shown in Figure 4.23, the resist pattern is first
transferred to a 1 µm layer of polysilicon and then to thick oxide. No separate steps
are required to remove the polysilicon mask as it is completely etched away in the first
deep RIE step.
Figure 4.23 Intermediate Polysilicon Layer for High Aspect Ratio Oxide Etch
4.6.1.8 Mask 2 Process Flow

Figure 4.24 explains the process flow for the second mask. The first step is to protect the Mask 1 structures using thermal oxide. The second mask structures, which include the spring, spring supports and the honeycomb features on the mirror block, are then patterned as shown in Step 2 of Figure 4.24. The spring is thinner than the honeycomb structure on the mirror because the honeycomb structures need to be wide enough to electrically connect the two levels on the movable fingers. The lower level of the mirror also provides mechanical support to the lower level actuators. Once the pattern is transferred to oxide, the first deep Silicon RIE step creates the spring in Step 4. The spring is released in Step 5 after sidewall passivation and extension etch. The extension etch is as far as the total height of the two level beams in the first mask.

The mirror structure is also released in Step 8 after another sidewall passivation and extension etch. Thermal oxide is used for sidewall passivation because it is totally conformal. The release step is long enough to release the lines on the mirror structure. The shadow of the spring that is created during the extension etch is also released during this step because it is a much thinner line.

The mirror is still attached to the floor by a thin oxide web which is removed by a short BHF dip. The final structure is shown in Step 9. The BHF dip should be short enough not to damage the vertical isolation segments. Note that there is another two level structure created on the mask on the spring and mirror. These are total overlap structures where a release step, rather than a thermal oxidation step differentiates between beam widths. This technique has been shown to create total overlap Z actuation [11].
1. Thermal Oxidation to Protect First Level Structures

2. Pattern Second Mask Structures
Spin Thck Resist and Pattern Second Mask Structures on Top Level Oxide

Figure 4.24 Two Mask Front Side Process Flow: Mask 2
Figure 4.24 (Continued)

3. Pattern Transfer to Oxide

4. Deep Si Etch: Form Spring

Protected by Oxide
Figure 4.24 (Continued)

5. Extension Etch & Release

Release Spring, Undercut Mirror

Protected by Oxide

6. Thermal Sidewall Oxide
Figure 4.24 (Continued)

7. Floor Clear
   DO NOT Clear Mask 1 Floor

8. Extension Etch & Release
9. Short BHF Dip

DO NOT etch away Vertical Isolation

Released Mirror & Spring

FINAL DEVICE CROSS SECTION
4.6.2 Single Mask Front Side Process Flow

The two mask process requires spinning thick photoresist on a released high aspect ratio structure on the second mask. It is not easy to protect released structures this way given the spin speeds, wet processing and step heights involved. Using a second mask is also expensive and makes the process more complex.

A simpler solution is to have the mirror structure and spring in the first mask itself. We impose the additional constraint that the width of the spring, the mirror honeycomb lines and all moving support structures should be equal to the width of the thin fingers on the Z actuator. With this condition, the upper levels of the spring, mirror and movable comb fingers and movable support structures would be released and oxidized through on the first level. The process flow would be exactly the same as in Figure 4.21 but without the short overlap segment. The lines on the movable support structures, mirror and spring would resemble exactly, the thin comb fingers in the process flow. The electrical connection to the movable fingers would be through the lower silicon level of the mirror and spring to the substrate.

The single mask device will have two independent suspended levels. The top level would be oxide and the bottom level would be silicon with thin oxide on the sidewall. Since the two levels are not mechanically connected, the top level would need to be etched back and removed with a long oxide etch step in the end. This is also the reason why the overlap segment cannot exist. If the overlap segment is formed, then it will not be mechanically connected to the lower level. A short oxide etch in the end is required in all versions of the process flow to expose the silicon on the top so that contact can be made to the bonding pads. The oxide etch in this case should be long.
enough to etch away the entire top level. Oxide etching should be done using an RIE tool because directionality is required. A BHF etch will etch away the vertical isolation segments and hence cannot be used.

**Single Mask Front Side Process**

**Structures After Mask 1 Process Flow**

![Diagram of Structures After Mask 1 Process Flow](image)

**Top Level Oxide Etch Back**

![Diagram of Top Level Oxide Etch Back](image)

Figure 4.25 Single Mask Front Side Process: Oxide Etch Back and Isolation
The modified final process steps in Mask 1 are shown in Figure 4.25 along with the electrical isolation details. Etching off the top level oxide has the added advantage that the spring is only half the actuator height. This process hence allows lower stiffness on springs and lower operating voltages. Since the lines on the mirror are the same width as the movable fingers, the mirror will also be on the lower level. A lower level mirror rotating around a lower level axis may or may not be suitable for the desired application of the device. Additionally, bonding a flat mirror might be the only way to make a mirror on the device. Filling in the holes with oxide and polishing the surface might be difficult on the lower level. Figure 4.26 shows a 3D schematic of the single mask device with the mirror, spring and suspended support structures on the lower level.
4.6.3 Front Side / Back Side Process Flow

4.6.3.1 Motivation

While the two mask process requires patterning thick resist across large steps and precise alignment between mask levels, the single mask front side process puts the mirror and the torsional axis on the lower level. Both processes also have a long thermal oxidation step after the first level structures are released. This step makes the vertical isolation neck and optionally also oxidizes the thin fingers through at the same time. The released structures are very compliant because the mirror, support arms and comb fingers are all anchored only at the spring ends. When such a large released structure is oxidized, the stresses due to volume expansion and thermal mismatch will cause extensive deformation. The warping effect can be large enough to destroy the device.

If the line width on all the suspended support structures for the mirror and comb finger banks is made equal to the width of the fixed fingers and the bonding pad, then only the thin fingers will be of smaller width. Since the first level release is timed for the smaller line width, the support structures will still be attached to the substrate during the long oxidation step after release. Only the thin comb fingers will be suspended during Step 10 on the Mask 1 process flow. The moving structure will hence be rigid enough not to warp significantly during this step.

Front side release of the device is now impossible. At the least, the bonding pads connecting to the wider fingers have to be attached to the substrate so as to provide mechanical support and to ground the bottom level of the wider fingers. The lines on
the bonding pad structures have to be of equal or lesser width than the lines on the moving support structures because the oxidation step needs to electrically isolate the two levels on the bonding pad and doesn’t necessarily need to isolate the two levels on the moving structure. The bonding pads will have the same etch via size as the support structures. Releasing the moving structure from the front side will hence release the bonding pads too. The solution is to release the device from the backside with a window that protects the bonding pads.

Backside alignment requirements will not be as critical as aligning two front side masks because the backside etch window is quite large. The placement of the bonding pads can also be used to control the required alignment tolerance. Additionally, since the backside etch holes are large, it is possibly to further simplify processing. The backside etch mask can be exposed on a separate wafer and etched through to create a stencil. Rather than doing backside lithography on the device wafer, the stencil can be aligned to the wafer. An oxide etch will transfer the pattern to the backside thermal oxide on the device wafer that is present as a result of front side processing. The oxide mask is used in the deep RIE tool to open up the release holes. Backside lithography and wet processing on a released device are hence totally avoided by using a stencil.

Another clear advantage of releasing moving structures from the backside is that the mirror can be a solid block. There are no steps that require filling the mirror honeycomb with oxide or subsequent polishing. Since the mirror is integrated with the actuator, no bonding steps are required to attach an external mirror like in the previous process flows.
Figure 4.27 shows a mask pattern for this process. The rectangle in the center is on a separate layer and is the backside etch window on the stencil.

4.6.3.2 Process Flow Description

The process flow is the same as the Mask 1 process flow shown previously. After the Mask 1 devices are fabricated, the stencil is used for backside release. As this version of the process has several advantages, it is described in full detail in this section.
1) MASK OXIDE GROWTH

3 µm thermal oxide, 1100°C, Wet, 17 hours 56 minutes.

2) AMORPHOUS Si DEPOSITION

1 µm amorphous Si deposition, 585°C, Stanford Nanofabrication Facility (SNF), hard mask for oxide etch.

3) LITHOGRAPHY

1 µm thick SPR 955 photoresist, expose and develop front side pattern.

4) MASK OXIDE ETCH

Amorphous Si etch followed by mask oxide etch, both on multi-chamber p5000 tool at the SNF with 20 seconds over etch in each case to ensure cleared floors in dense areas.

5) DEEP Si RIE #1

12 minutes subr_k04 custom batch process on Bosch tool. RIE power: 0.1 W for deposition and 9W for etching. Step times: 1 second deposition, 2 seconds etch ramp, 1 second etch. Step times are shortened to obtain sidewalls with roughness much smaller than line width. Etch depth: 25 µm.

6) SIDEWALL OXIDATION

150 nm thermal oxidation at 1100°C, Wet, 5 minutes 36 seconds for passivation prior to release. No significant change in mask oxide thickness.
7) FLOOR CLEAR

40-45% over etch to account for loading in dense areas. This step removes approximately 210nm off the mask, leaving 2790 nm mask oxide.

8) RELEASE #1

subr_k11 custom batch process on Bosch tool. 3 - 6 minutes depending on targeted line width and via size. No deposition-etch cycling. 5 seconds pre-deposition, 35W RIE etch power, 15mT pressure to release thin lines and to yield necks of 1 µm or less on wider lines.

Even though fixed finger support structures, fixed finger bonding pads, and fixed fingers are all same thickness, one-dimensional loading will cause all fingers to release. Two-dimensional loading on tight etch vias will reduce etch rate therefore allowing support structures and bonding pads to remain fixed to substrate. Release time depends on the finger gap in the targeted design variant since bigger finger gaps will allow less loading on fingers and will also yield greater etch rates in vias, since the etch via size scales with the finger gap. The devices with 2.5 µm, 3.5 µm and 5 µm finger gaps will have 5 x 6 µm vias, 5 x 8 µm vias and 5 x 11 µm vias respectively. Release before thin finger oxidation reduces vertical gap because smaller line width reduces time needed for release and therefore the vertical etch distance as well. Figure 4.28 shows the device cross section at this stage.
9) **THIN FINGER / NECK THROUGH OXIDATION**

3 hour oxidation, 1100°C, Wet to fully consume 1 μm thin fingers and necks simultaneously. This step will grow about 1200 nm of floor oxide and will increase mask oxide back up to 3000 nm. Springs will be partially to fully oxidized, depending on their thickness. Compliant spring ends as discussed earlier will eliminate buckling of springs. However, this will only work if the spring and spring brackets are released prior to oxidation. If not, they will be fixed to the substrate and will therefore be unable to accommodate oxidation and thermal expansion induced strain.

Fixation of the thick and thin finger support structures to the substrate will prevent both in-plane and out-of-plane buckling during oxidation and will also eliminate differential shrinkage during cooling therefore
eliminating finger shifting. Figure 4.29 shows the cross section at this stage.

![Cross Section Diagram]

Figure 4.29 Etch profile after Long Thermal Oxidation in Step 9

10) FLOOR CLEAR

40-45% over etch. The step will remove around 1700 nm of oxide from the mask, leaving around 1300 nm.

11) DEEP Si RIE #2

12 minutes subr_k04 custom batch process on Bosch tool. RIE power: 0.1 W for deposition and 15 W for etching. Step times: 1 second deposition, 2 seconds etch ramp, 2 seconds etch. Lower level etch needs to be more aggressive than the upper level etch because the gaps are smaller and trenches are deeper at this stage and the etch will taper and close the gaps if it is not more aggressive than the first level etch.
12) SIDEWALL OXIDATION

100 - 150 nm oxidation for sidewall passivation prior to release. No significant change in mask oxide thickness.

13) FLOOR CLEAR

50 - 75% over etch to account for increased loading in the deeper floors and narrower gaps. Approximately 1 µm mask oxide remains.

14) RELEASE #2

subr_k11 custom batch process on Bosch tool. 5 - 8 minutes depending on targeted line width and via size. No deposition-etch cycling. 5 seconds pre-deposition, 35W RIE etch power, 15mT pressure to release thin lines and to yield necks of 1 µm or less on wider lines. We need the release extent to be similar to Release #1 (Step 8). Release of fingers followed by subsequent short oxidation (Step 15) will allow for thinning of the finger support structures and mirror during back etching without affecting the fingers themselves. If the necks on the wider lines are too narrow then we will not be able to remove much material during backside thinning due to shadow masking by the neck sidewall oxide. If they necks are too wide, then we will remove too much material therefore potentially compromising structural integrity.

Back side thinning would not be possible if the fingers are not released and protected first because we would thin down both fingers and springs as well, which would adversely affect device performance.
15) SHORT OXIDATION

100 – 300 nm oxidation to protect bottoms of released fingers during subsequent backside etch.

16) OPTIONAL FLOOR CLEAR

50 – 75 % over etch to account for increased loading. Approximately 700 nm of mask oxide remains. Figure 4.30 shows the cross sections at this stage.

![Figure 4.30 Device Profile after Front Side Processing](image-url)
17) BACKSIDE OXIDE AND POLY ETCH

About half the amorphous silicon on the backside would be consumed due to the thermal oxidation steps during front side processing. The result is an oxide – Si – oxide layer on the backside with approximate thickness 1 µm – 0.5 µm – 3 µm. The 3 µm oxide layer is the innermost layer. The first two layers can be etched with or without a stencil and a long over-etch is acceptable. A backing wafer with a recess is used to protect the front side devices. A recess is easily created on a standard wafer by etching a blank wafer on the Bosch tool. The clamp that holds the wafer down on the Bosch tool will mask an outer ring on the wafer and will create a large slot on the rest of the wafer.

18) BACKSIDE MASK OXIDE ETCH

The stencil wafer is placed on the back of the device wafer and a backing wafer similar to the one described in Step 17 is placed on the front side of the device wafer. The stencil wafer is used to pattern the mask oxide on the backside after alignment. Depending on the alignment accuracy required, a simple alignment of the flats by hand might work.

19) BACKSIDE DEEP Si RIE RELEASE & THINNING ETCH

The Bosch is used to deep etch cavities from the backside using the oxide mask. The oxide floor on the front side acts as an etch mask to protect the actuators. The backsides of the mirror and support structures are still exposed and should not be etched away but can be
thinned down to reduce the moving mass. This feature allows a certain
degree of flexibility on the timing of the backside Si etch. Figure 4.31
shows the final cross sections.

Figure 4.31 Final Device Profile

20) BACKSIDE REMNANT OXIDE ETCH

The remaining oxide webs on the device will need to be etched away
with a short BHF dip.
4.6.3.3 Potential Problems

1) Multilevel Tall and Composite Springs

The upper level of spring will be nearly or fully oxidized and released from the lower level, which will be mostly silicon. The spring is also as tall as the rest of the device. This may affect the strength and stiffness of the spring, which may therefore change the maximum tilt angle and resonance frequency. It is possible to overcome this problem by using springs that will oxidize through on the top level. A long oxide etch back in the end will etch away upper level oxide structures.

2) Increased Moving Mass

The mirror is solid and will be the same height as the springs and actuator and therefore more massive relative to the first generation designs. The increased mass would lower the resonance frequency. The mass, however, is concentrated near the axis of rotation and hence may not affect the system significantly. Step 19 can be used to control the mirror mass in order to tune the frequency.

The free finger support structures will also be more massive due to thicker line widths. The majority of this increased mass is located near the end of the lever arm and may significantly lower the resonance frequency. Step 19 can be used to control the mass of the support structures too.
3) Backside Etch Non-Uniformity

The backside etch step is a long step on the deep Si RIE tool. The etch takes between 2 and 4 hours depending on the thickness of the mask oxide on the backside and the etch recipe used. The etch has to go through approximately 450 µm of silicon in a window that is roughly the same size. The corners of the window will be etched at a slower rate than the center of the window. Though this effect is not very pronounced due to the large size of the window, it becomes significant for large etch depths. The maximum allowed difference in height between the backside of the mirror and the actuators is 25 µm for a 50 µm tall device. If the height difference is larger than this value, the lower level of the mirror will be etched away before the actuators are exposed and the electrical ground on the moving comb fingers will not be achieved. Figure 4.32 illustrates this issue.

There is another issue with backside non-uniformity. Given that there is always a non-zero alignment error between the backside etch windows and the front side devices, the mirror will never be exactly at the center of the window. For a general alignment error in two dimensions, there will be one corner of the actuator that is closer to a corner of the window. The opposite corner will open up before this corner and this will result in one section of the actuator bank and support structures being etched away faster than the other areas. Figure 4.33 illustrates this issue.
Releasing the comb fingers from the front side and protecting them with oxide prevents etching of the comb fingers from the back and allows a long over etch on the comb finger backside. The support structures, however, are not protected, because they cannot be fully released from the front side. The lower level of the support structures is hence in danger of getting etched away. The bigger problem, of course, is the mirror because it is close to the center of the etch window.
The backside etch recipe can be made straight, tapering or reentrant. A tapering recipe makes the etch window effectively smaller. This means that the non-uniformity is concentrated in a smaller area. This is detrimental to the device. A reentrant etch makes the etch window larger and spreads the non-uniformity across a larger area, resulting in a greater likelihood of releasing the device properly. When using a reentrant etch, it should be ensured that the etch windows on neighboring devices do
not overlap, as this might release the spring supports. In the other direction, bonding pads might be released if the etch windows are too large.

A possible solution to the problem with non-uniformity is to thin down the backside of the wafer first before doing the stencil etch. With a shorter etch depth through the backside etch window, the difference in etch depth between the center of the etch window and the edge will be not be as much. Depending on how thin a wafer the tools can handle, this method might help etch away the backside of the actuators before the lower level of the mirror has been etched away. Figure 4.34 illustrates this modification.

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**Figure 4.34**  Back Etch after Wafer Thinning Increases Uniformity
For the process sequence that includes wafer thinning, the oxide and polysilicon layers on the back of the wafer should first be etched away without a stencil mask. The wafer is then thinned down to about 100 µm with a deep silicon RIE step. 1 µm PECVD SiO₂ is deposited on the backside and the stencil is used to pattern the oxide. The non-uniformity within the windows is minimal at this stage because the non-uniformity during this thinning step is distributed over the entire wafer instead of just the etch windows. The deep RIE tool is used once again to etch within the windows. The etch depth now is only 100 µm rather than the 500 µm for a standard wafer and the uniformity is much better.

4.7 Mask Design

4.7.1 Introduction

The mask layout is created to cover most of the design space that will yield useful results. Mask layout is done in Mentor Graphics IC Station. All lines are drawn as paths with non-zero width. All path intersections are three way intersections. Four way intersections take longer to release for a given line width and trench size and are avoided. The masks include a subset of the following design space:
Moving Finger Width 0.5 µm – 1 µm
Fixed Finger Width 2 µm – 2.5 µm
In-Plane Finger Length 20 µm – 30 µm
Finger Spacing 2 µm – 5 µm
Mirror Size 50 µm – 200 µm
Torsion Spring Width 1 µm – 3 µm
Torsion Spring Length 50 µm – 200 µm
Torsion Spring Height 10 µm – 50 µm
Spring Ends U Shaped, Butterfly

The torsion spring height is not a design feature, but actually a process feature that depends on how many masks are used and the height of the actuators. The number of comb fingers depends on the other geometrical parameters in the design space, because the comb fingers are used to fill in the entire length taken up by the mirror, spring and supports. There is one design variant on the comb finger count that has multiple finger banks. Multiple finger banks mean that the comb fingers are effectively farther away from the spring and require lower force and large displacement for a given tilt angle. The required voltage is further lowered due to the large number of fingers present.

The mask also includes simple test structures to calibrate the various stages of the process. Both the single mask and the two mask front side devices are on the same mask. For the single mask device, only Mask 1 is processed, while both masks are processed for the two mask device.
4.7.2 Single Mask and Two Mask Front Side Process Masks

Figure 4.35 shows the overall mask layout imported from IC Station. The layout covers several design variants as discussed previously. The die takes up roughly 14 mm space on the wafer.

Figure 4.35 Mask Layout as Imported from IC Station: Mask 2 Overlaid on Mask 1
Figure 4.36 shows the first mask pattern on the two mask device. Note that the mirror, spring and spring supports are not patterned in Mask1 and are represented by the large block in the center. There are actuators and bonding pads on each side of this block. The details on the actuator banks and bonding pads are not shown.

Figure 4.36  Mask 1 pattern on 2 Mask Device: Imported from IC Station

Figure 4.37 shows the second mask pattern on the two mask device. Note that the first mask devices are protected while patterning the second mask.

Figure 4.37  Mask 2 Pattern on 2 Mask Device: Imported from IC Station
Figure 4.38 and Figure 4.39 show single mask, single pad and multi-pad devices. The mirror structure, spring, actuators and bonding pad are patterned in the same mask.

Figure 4.38  Single Mask Device: Imported from IC Station
Figure 4.39  Single Mask Multipad Device: Imported from IC Station
4.7.3 Front Side / Back Side Process Masks

There is one front side mask for the devices and a separate mask for the stencil. The design space covered is similar to the previous case, except that there are more variants on the spring width and fewer variants on the mirror size. Figure 4.40 shows the overall layout of the mask.

Figure 4.40  Mask Layout: Front / Back Side Process: Imported from IC Station
Figure 4.41 shows a device that has 1 \( \mu \text{m} \) thin fingers, 2.5 \( \mu \text{m} \) thick fingers, 3.5 \( \mu \text{m} \) finger gap, 20 \( \mu \text{m} \) finger overlap, 1.5 \( \mu \text{m} \) spring width, 100 \( \mu \text{m} \) spring length and a 100 \( \mu \text{m} \) mirror. The box in the center is the overlaid stencil etch window.
Figure 4.42 and Figure 4.43 show close up pictures of the device and the folded “butterfly” spring.
Individual devices on the mask layout are labeled with an alphanumeric code to determine the sequence. They are also labeled and with the details of the geometry variance on each device. A portion of a mask layout is shown in Figure 4.44 with the codes and the geometry details. The resolution strip and the vernier scale are in the middle of the mask. The vernier scale is used to measure the alignment error between the two masks after the device is fabricated.
<table>
<thead>
<tr>
<th>Device</th>
<th>m</th>
<th>g</th>
<th>Device</th>
<th>m</th>
<th>g</th>
<th>Device</th>
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<td>20</td>
<td>A2</td>
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<td>20</td>
<td>A3</td>
<td>100</td>
<td>20</td>
<td>A4</td>
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<td>20</td>
<td>C2</td>
<td>100</td>
<td>20</td>
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<td>2.5</td>
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</tbody>
</table>

The table describes for each device, the mirror size (m), thin finger width (f), finger gap (g), finger overlap (O), spring width and length on each side of the mirror (s). The suffix on the spring specifications is for variations in spring bracket design.
4.8 Conclusions

Mechanical, electrical and process design were demonstrated for a micromirror device for possible applications in display devices and optical switching among others. The mirror is suspended by a torsional spring and is attached to Z directional comb actuators. Of the various Z actuator designs discussed in previous chapters, the partial overlap design and the non-overlapping design were chosen for their advantages in constant force and large range of motion for a given etch depth. While total overlap Z actuators have been proven to work, the partial overlap process is more complex and needs to be proven.

The performance specifications of the micromirror device were listed in terms of the response time, resonance frequency, angular displacement and size. Design considerations and trade offs were discussed including the corresponding constraints on geometry and process parameters. Examples of design trade offs include conflicting requirements on stiffness for the angle of twist and resonance frequency. Such trade offs were solved to get an acceptable performance.

Electromechanical design issues were discussed and analytical and numerical design computations were shown. Frequency and displacement analysis for torsional and in-plane modes, along with stress analysis were used to arrive at a set of usable geometries. These geometries allow the required torsional twist and frequency while separating the in-plane mode from the torsional mode. The presence of the mirror as a rigid block on the torsional spring was found to help in separating the frequencies of the first two modes. Spring end modifications for process stress issues were also
discussed. The “butterfly” design was found to take the compressive stresses during thermal oxidation while preventing buckling of the released spring.

The process design sections described the single mask and two mask front side process and the front side / back side process together with the advantages and disadvantages of each. While single mask processing is preferable for the sake of simplicity, there are a few disadvantages such as a lower axis of rotation and stress induced warping on these devices. Due to stress issues associated with long thermal oxidation steps on compliant released MEMS, the most workable version so far seems to be the front side / back side process, where the devices are all made on the front side while the support structures are attached to the substrate and then released with a stencil on the back side. The process does not require fine alignment or a second lithography step. Alignment and stress issues may however still prove to be detrimental to the device. Electrical and mechanical isolation issues were also discussed. Based on the process flow diagrams, process constraints were listed and were used to fine tune the useful design space.

Mask layout was described for all the three possible process flows shown. The die takes about 14mm of space on the wafer and has 60 to 80 devices per die depending on the layout. The devices on the mask are designed so as to cover the entire useful design and process space as calculated in this and preceding chapters.

The next chapter details the processing results obtained on the micromirror device. The process flow for the single mask front side process and the stencil based front side / back side process are shown in parallel because they have several steps in common. The processing was done as a team effort given its complexity.
References

[1] Ding, Ko, Mansour, Mechanical Properties of Single Crystal Silicon


5.1 Introduction

This chapter describes the fabrication results for the micromirror. Electromechanical design, process design and mask design were described in previous chapters. Several design variants are laid out on the mask pattern. The process flow parameters for any particular run depend on the targeted design variant. For example, a particular choice of process parameters in the release steps would only work for a set of devices with a certain finger width, spring width and finger gap. Process flow is based on the partial overlap and non-overlapping Z actuator designs as partial overlap actuators yield superior performance compared to total overlap actuators. Though total overlap actuators have a simpler process flow, their performance characteristics are insufficient for the micromirror device.

Both front side and back side process flow results are described in this chapter. We first start with the front side process flow and describe lithography, oxide patterning, first level deep etch, first level release, two level structure formation, isolation neck formation, second level deep etch and second level release. The problems and issues with front side process flow are described. The front side / back side process flow is shown to alleviate several of the problems described. Finally, back side processing results are shown and alignment issues with the backside process are discussed.
The processing results shown here are specific to the micromirror device and follow the process flow diagrams shown in the previous chapter. The process is an extension to the basic two level process and includes a combination of thermal oxidation based line width differentiation with shadow masking and vertical isolation using narrow necks.

5.2 Front Side Processing Results

5.2.1 Wafer selection

Highly doped p+ wafers are used because structural silicon is used as the conducting material. Standard 4” <100> wafers are used. <100> wafers are used so that KOH etch steps can, if necessary, be used to create large sidewall faceting at a later stage. KOH etching stops at the <111> plane and creates sidewalls that are far more faceted than what is possible by profile control in the Bosch etcher. 4” wafers are chosen for compatibility with the clean room tools. Additionally, for the die size used in the mask layout, about 5 die can fit on a 4” wafer. A 5 x 5 array of chips is useful for calibration during various stages of the process. A box of 25 wafers is taken through the process flow. Both individual devices and whole wafers are sacrificed for calibration along the process.
5.2.2 Mask Oxide Growth

3 µm of thermal mask oxide is grown on the wafers. Wet oxidation at 1100°C is done for all thermal oxidation steps in the process. Silicon dioxide flows at that temperature and residual stresses in the device are lower. Thermal oxidation steps are very predictable and no characterization is required at this stage.

5.2.3 0.5 µm Lithography

The first generation of devices had 0.5 µm movable fingers. The small width on the movable fingers reduces thermal oxidation time and consequently reduces the stress issues associated with thermal oxidation. Small finger width also reduces the first level release time and hence the vertical gap. However, it is difficult to maintain the integrity of 0.5 µm features over large depths.

Lithography is tuned for a 0.5 µm minimum feature size and 2.5 µm minimum gap. The resolution limit of the stepper at the UC Santa Barbara clean room is 0.5 µm lines and spaces. However, because of the larger gaps we have to work with, it is possible to achieve repeatable features at the line-width resolution limit. Overexposure helps reduce line width at the cost of increasing the gap, thus providing an additional dimension of control in the lithography.
SPR 955 photoresist gives fine lines and spins to about 1 µm thickness at 3000 rpm.

The following recipe is used for resist coating:

1. Solvent clean: Acetone, Iso Propyl Alcohol (IPA)
2. Dehydration bake: 100°C, 3 minutes. Cool 3 minutes
3. HMDS Primer: Coat and wait for 15 seconds, Spin 3000 rpm, 30 seconds
4. SPR 955 photoresist: 3000 rpm, 30 seconds
5. Pre-Bake: Hot Plate, 100°C, 90 seconds. Cool 1 minute
6. Optional CEM 365 (Contrast Enhancement Material): 3500 rpm, 30 seconds
7. Expose on 5X Stepper with 5X Chrome mask (typically 1.1 seconds)
8. Post Exposure Bake: 110°C, 90 seconds
9. If CEM is used, wash CEM away with DI water
10. Develop: MF 701, 75 seconds with occasional mild agitation
11. DI rinse for 2 minutes, purge DI, rinse again for 2 minutes
12. Soft N₂ blow dry

The photoresist spin step is not very tolerant to contaminants in the resist. Such contaminants leave streaks and patches on the wafer after spinning. This problem is solved to a large extent by ramping up the spin speed during the first 10 seconds and spinning at 3000 rpm for the rest 20 seconds. That way the heavier particles are pushed out of the wafer before the resist dries. Figure 5.1 shows a 0.5 µm feature made using this process. The SEM does not give good pictures of photoresist on oxide because the wafer surface is all dielectric. Figure 5.2 shows repeatable 0.5 µm lithography with 0.5 µm and 1 µm lines and 4 µm spaces.
Baking parameters, especially temperature, can be used to modify the sidewall profile of the photoresist. The profile should be as vertical as possible so that a faithful pattern transfer to oxide is also vertical. The lithography parameters presented are optimal for SPR 955. Figure 5.3 shows a tapering resist profile caused by higher baking temperature. Such a profile can also be caused by incorrect focus settings.

Developing parameters do not seem to have a significant effect on the pattern. The DI rinse after the develop step is very important in that it should be long enough to clean the wafer of residual photoresist very well.

Figure 5.1 0.5 µm Lithography: Feature Measures 517 nm
Figure 5.2  Repeatable 0.5 µm Lithography with 4 µm Spaces
Lines shown are 560 nm and 1.05 µm

Figure 5.3  Tapering Resist Profile: Incorrect Focus and/or Baking Temperature
Feature Size Tapers from 321 nm to 582 nm
A focus / exposure test is used to find the optimum focus and exposure settings for the stepper under current conditions. A device array is exposed for the purpose, wherein the exposure is swept on the horizontal axis and focus is swept on the vertical axis. Exposure is tuned predominantly for feature and gap size while the focus is tuned for sidewall resist profile. A typical exposure time for SPR 955 is 1.1 seconds. This number could change from run to run.

While exposing the wafer in the stepper, it is important to align the mask using the fiducials and also to align the wafer to the screws on the chuck. This is all the more important for the front side / back side process where the stencil wafer that is used for the back side etch will also be aligned to the same screws on the chuck before it is exposed with the stencil mask and will eventually be aligned to the back side of the device wafer.

When exposing a large batch of wafers it is important to recalibrate the exposure and focus settings every few wafers because of the intensity drift in the lamp. Figure 5.4 shows a pinched off 0.5 µm comb finger due to an uncalibrated focus setting.
5.2.4 Oxide Etching

The oxide etch process is calibrated to maintain straight sidewalls on 0.5 µm features while preserving the integrity of the 3 µm mask oxide. This means that high selectivity, fine features, high aspect ratios and straight etch profiles are important requirements at this step. Thin photoresist is used to pattern the fine features. A standard oxide etch that uses CHF$_3$ and O$_2$ is made very selective to photoresist by reducing the O$_2$ flow to near zero. The 3 µm thermal oxide mask is entirely preserved during the etch but the sidewall is very tapered as shown in Figure 5.5. Such tapered sidewalls are characteristic of CHF$_3$ recipes.
CF₄ chemistry is used as an alternative means to etch the oxide. An etch recipe that uses 25 sccm CHF₃, 50 sccm CF₄, 100 sccm Ar with 250 W RF power and magnetic field of 60 Gauss at 23 mT pressure in the p5000 etch tool is found to yield very straight sidewalls. The selectivity of this recipe to photoresist is very low and the remaining mask oxide thickness after this step is much less than 3 µm. This necessitates the use of an intermediate hard masking layer as described in the previous chapter. Polysilicon is used for hard masking because metals are incompatible with most equipment in the clean room and polysilicon can be automatically removed in the first deep Si RIE step.
In the first experiment, 1 µm of polysilicon is deposited at 610°C. Photoresist is difficult to spin on these wafers because of the rough surface. With a ramped resist spin and 0.5 µm lithography, the resist is hard baked at 110°C for 30 minutes. The polysilicon is first etched away with the resist mask. An end point detection algorithm with an additional over-etch is used to etch the polysilicon. An over-etch that is larger than required causes faceting in the poly layer. Sidewalls are less faceted than the CHF₃ oxide etch at this stage, but the floor is extremely granular, causing jagged edges on the comb fingers.

Figure 5.6  Photoresist on High Temperature (610°C) PolySilicon

Rough Floors and Rough Sidewalls on Small Features

Figure 5.6 shows photoresist on the rough poly surface with jagged edges. A deep Si etch at a later stage results in badly formed beams. The rough edges cause certain parts of the line to be thinner than others and these smaller widths cannot be faithfully
carried through to a large depth. The result is a set of visible gaps in the thinner beams that correspond to the thin sections of the poly and oxide caused by the rough sidewalls, as shown in Figure 5.7. The mechanical integrity of these beams does not last until the first oxidation step. Their increased compliance causes in-plane warping as in Figure 5.8.

Figure 5.7 Rough Edges on Fine Features Affect First Deep Si Etch
Figure 5.8  Rough PolySilicon Causes Warping in Thin Features

Figure 5.9  Oxide Height Differential based on Line Width
The poly and oxide etch steps have a loading effect that results in thinner lines etching more aggressively than the wider ones. Figure 5.9 shows the reduced oxide thickness between fingers of different widths. This is not a problem as long as the finger lasts until the long oxidation step when it is fully consumed. Small defects in the thin fingers will be covered up at this stage and there will be a very tall oxide mask for the lower level. There is also a notching effect caused by the poly and oxide over-etch [1]. The notching effect happens when a silicon etch step strikes a buried oxide layer. Charging of the oxide layer causes the ions to be deflected sideways. The polysilicon etch with photoresist mask can either be done in the Bosch etcher or in the p5000 tool which uses Cl₂ and HBr. The Bosch etcher is extremely aggressive and has exaggerated notching effects. Figure 5.10 and Figure 5.11 show a case where the Bosch etcher was used to etch the poly and only three way intersections have any silicon left. Thin comb finger lines are way too thin to transfer effectively to oxide.
Figure 5.10  Poly Etch on Bosch Tool Too Aggressive: Removes Thin Fingers

Figure 5.11  Bosch Poly Etch Preserves Only 3-Way Intersections
Figure 5.12 shows the notching effect caused by a Bosch etch at the buried oxide layer. This effect releases the thin beams during the oxide etch step. Since the Bosch tool etches very fast, even a short over-etch of a few seconds is long enough to damage the device.

Lower temperature polysilicon deposition was found to yield a much smoother floor and consequently smoother sidewalls on the thin fingers. Figure 5.13 shows polysilicon deposition results at 585°C. The Figure shows photoresist lines on polysilicon.
The subsequent poly etch is done in the p5000 tool using 20 sccm Cl$_2$ and 20 sccm HBr with an RF power of 200W and a magnetic field of 40 Gauss at a pressure of 100 mT. When an over-etch of 20 seconds beyond the end point is used, this recipe yields fairly straight sidewalls on poly. There is a small amount of faceting and a short notch at the top. Figure 5.14 and Figure 5.15 show 1 µm and 0.5 µm comb fingers respectively after the Cl$_2$ / HBr poly etch and the CHF$_3$ / CF$_4$ / Ar oxide etch. There is very little poly left on the lines due to the approximate 3:1 selectivity of the oxide etch recipe to poly.
Figure 5.14  3:1 Aspect Ratio Lines in Oxide: 1 µm Feature

Figure 5.15  6:1 High Aspect Ratio Lines in Oxide: 0.5 µm Feature
5.2.5 First Level Deep Silicon Etch

Since the integrity of the mask oxide is a critical issue in SCREAM-like process flows, all silicon etch recipes are tailored to the extent possible for high selectivity to oxide. Chlorine chemistry in deep Silicon etching can be used to give very smooth and straight sidewalls. The process, however, is not very selective to oxide, with selectivities on the order of 10:1 only. The Bosch process, however, has a selectivity of about 133:1 to oxide when a deposition etch cycling process is used at 9W RF power with 40 sccm Argon. This is partly because the deposition of the passivating material over the oxide mask causes the mask to be etched only when the passivation has been removed at some point in the etch step of the cycle. When pure SF6 is used in release steps, selectivities are much lower. Higher power and higher Argon flow both contribute to faster physical etching and hence lower selectivity to the mask. The Bosch process is a fast etch process for silicon and is the choice for deep Si RIE.

The deep Si etch has to be tuned for the finger gaps in the targeted design variant. We first create a recipe that reduces sidewall roughness to the extent possible because the roughness cannot be on the order of line width if the structural integrity of the comb finger has to preserved and the comb finger has to remain a continuous line. Since the Bosch process works by cycling deposition and isotropic etching steps, the solution is to reduce the deposition and etch time by the same factor. That way the scallops created at each step are smaller than normal. The fact that the scallops are nearly isotropic means that smaller scallops translate to lower etch rate in all directions. Lower lateral etching at each step translates to reduced sidewall roughness. It was found that deposition and etch times could be made as low as 1 second each. There is an etch ramp of 2 seconds between the two steps as in the standard process. At this
speed, the mass flow controller can barely keep up with switching the deposition and etching gases. The deposition and etch steps overlap while the gas flow rates stabilize and it is possible that the two processes are actually happening simultaneously. The result is a very smooth sidewall on a very high aspect ratio structure. Figure 5.16 shows a 1 µm spring etched 25 µm into the wafer. Sidewalls scallops are barely visible.

Figure 5.16 Smooth Sidewalls: Scallops Almost Invisible
The RF power used in the recipe depends on the etch depth and the gap. It is found that the 9W power in the standard Bosch recipe will suffice for a 5 µm gap etched down 25 µm. A 2.5 µm gap requires 12 W of RF power to get the same sidewall profile across the same depth as shown in Figure 5.17. A short notch is evident at the beginning of the etch. This notch is characteristic of the Bosch process with the oxide mask and causes the line width of the silicon beam to be slightly lower than the oxide line width.

![Image: Straight Sidewalls at 2.5 µm Gap: 12 W Power](image)

**Figure 5.17**  Straight Sidewalls at 2.5 µm Gap: 12 W Power

0.5 µm Features, 25 µm Deep, 50:1 Aspect Ratio

Using lower power in a smaller gap will cause trenches to narrow down or lines to widen slightly as shown in Figure 5.18 while using a higher power in a large gap will be too aggressive as shown by the compromised spring in Figure 5.19. The spring is surrounded by a large open space.
Gradually Increasing Line Width

Figure 5.18  Loading Inside Trenches Caused by Low Power Deep RIE

Figure 5.19  Structures in Open Spaces Etched Aggressively with High Power
It is difficult to get a repeatable high aspect ratio structure from a 0.5 µm beam. Slight changes in lithography and etch conditions affect the structural integrity of the beams. Portions of these beams are released and deformations are seen on long beams as shown in Figure 5.20. All 1 µm lines are intact. For that reason, it is probably advisable to do away with 0.5 µm line widths altogether despite the advantages with short oxidation times, fewer thermal oxidation related stress issues and smaller vertical gap. A single mask front side device with 1 µm thin fingers, processed until this stage is shown in Figure 5.21. The mirror appears as a honeycomb and the device label I6 is also seen in the micrograph. Figure 5.22 shows a front side / back side device with solid mirror at the same stage of processing.

Figure 5.20 0.5 µm Beams Sometimes Deform After First Deep RIE
Figure 5.21  Single Mask Front Side Device After First Deep RIE

1 µm Thin Fingers and Springs Intact

Figure 5.22  Front Side / Back Side Solid Mirror Device After First Deep RIE
5.2.6 Sidewall Passivation and Floor Clear

The finite etch rate of SF6 for thermal oxide combined with physical etching of the sidewall oxide requires that a certain minimum oxide thickness be used. Experiments with 100 nm sidewall oxide show that the passivation can fail when a high power release is used in narrow gaps such as 2.5 µm. 100 nm sidewalls are however sufficient for the first level release of 5 µm gaps. A thermal oxide layer of 150 nm is usually sufficient for any gap that can be Bosch etched reliably.

The floor clear step is done using a standard CHF₃/O₂ process step at 10mT and 450V. Loading is significant in narrow gaps. Experiments show that at least a 30% over-etch is required to fully clear the oxide floor in 2.5 µm gap devices. A larger over-etch will reduce the mask oxide thickness more than required.

An optional short deep Si etch of around 5 µm or more at this stage followed by an additional sidewall passivation and floor clear step can be used to make a three level partial overlap comb drive. The etch parameters for this step are similar to the previous deep Si etch, thermal oxidation and floor clear steps. If the partial overlap segment is created then the mask oxide is lower by about 200 nm and the spacing between fingers reduces by about 150 nm. If the overlap segment is omitted at this stage, then the process yields a non-overlapping Z comb drive.

5.2.7 First Level Release

The first level release step constitutes release of lines of smaller width. It coincides with the creation of the vertical isolation neck in the larger width lines. While it is
possible to oxidize the thin fingers through and create two level structures before release, post release oxidation combines the oxidation of the thin finger and the isolation neck into one step. It also reduces one floor clear step thus saving mask oxide. We hence pursue the variant of the process flow where both the thin comb fingers and the vertical isolation neck are oxidized through after the first level release. However, oxidizing the thin finger through after release means that an overlap segment cannot be created in the previous step. This is because the overlap segment has to be on a second level to aid in Z actuation. The smaller line widths on the first level have to be partly or fully oxidized through to differentiate them from the second level. If they are partially oxidized, the oxidation will have to be completed when the isolation necks are oxidized through such that there is some silicon left in the overlap segment.

As discussed in previous chapters, the release process has conflicting requirements on isotropic etching and loading. For a given lateral etch rate, the isotropic release process will have an equal vertical etch rate. A less isotropic etch will etch more vertically than laterally thus creating a larger vertical gap between levels to achieve a given size of the isolation neck.

The deep Si etch tool is used for the release process. Instead of deposition-etch cycling, there is one long SF$_6$ / Ar etch step. Since the plasma in the Bosch etcher is lit with deposition gases rather than SF6, there is a short pre-deposition of 5 seconds to help transition from the light step to the release step. A low RF power of 0.1 W with the ICP power maintained at the standard 825 W results in a very isotropic etch. The problem with this recipe is that the gaps between fingers which have one-dimensional loading and the honeycomb gaps which have two dimensional loading are etched with
respectively slower etch rates. Figure 5.23 illustrates this problem. The spring is fully released and so is the outer edge of the wide bar connecting the spring to the mirror. The inner lines on this bar are heavily loaded and take much longer to release.

Figure 5.23 Loading Effect During Low Power Isotropic Release
Release loading becomes a serious issue when there is a huge height differential between the spring and the mirror when all moving structures are eventually released. For the case shown in Figure 5.24, the gap below the spring is larger than the height of the spring itself. The spring will not shadow correctly on to the lower level in this case. Even if it does shadow, the lower level of the spring will be on a level that is entirely lower than the mirror. The comb fingers only have one-dimensional loading and they will be at an intermediate level between the mirror and the spring. The axis of rotation will hence be much below the device. If the spring does not shadow correctly as shown in Figure 5.25, then the top level oxide etch will etch the spring away and the suspended structures will have no mechanical support. Another issue is the large vertical gap at the comb fingers in spite of using an isotropic release recipe.
because the mirror honeycombs take longer to release thus over-releasing the comb fingers.

Figure 5.25 Incorrectly Shadowed Spring due to Large Vertical Gap

The solution is to use higher RF power at the cost of more anisotropic etching. The RF power is increased from 0.1 W to 35 W. The larger power gives the ions more energy to penetrate small gaps and reduces the loading effect to a large degree. A reduction in process pressure from 23 mT to 13 mT is also found to reduce the loading effect slightly. Figure 5.26 shows a support structure on the edge of the device that is released with the high power, low pressure recipe. The vertical gap is not very large even in the open spaces.
Since it is not easy to use an SEM to look underneath the honeycombs to prove release, we choose from two release test methods. If the entire movable structure is released as in this case, the structures are moved using a fine probe in the probe station. If the device moves as intended without breakage and also springs back to its original position when the probe is released after a short displacement, then it means that the release is complete. In an attempt to show the importance of the probe test method, the probe was used to carefully break off only the moving comb fingers, moving finger supports and mirror. Figure 5.27 shows a view of the fixed fingers with only the release shadows of the movable fingers. It can be seen that the vertical gap at the comb fingers is not very large.

![Figure 5.26 Low Release Loading with High Power](image)
Figure 5.27  Movable Fingers Broken Off with Probe to Show Release

The probe test method, however, cannot be used for the front side / back side process devices because all support structures are still connected to the substrate as in Figure 5.28 and will be released only after the back side etch. In this case, a large probe is used to destructively cleave the bonding pad on one device as in Figure 5.29. The bonding pad via size is the smallest via size in the device. The width of the bonding pad necks is an indication of release extent. If the bonding pad lines are more than 1 µm thinner in cross-section at the neck, then it can be safely assumed that 1 µm lines elsewhere on the device, whether comb fingers or honeycombs, are all released. Figure 5.30 shows a cleaved bonding pad when the device is over-released. The bonding pad necks are extremely thin.
Figure 5.28  Support Structures Not Released for Front Side / Back Side Device, Fixed to Substrate to Prevent Warping After Oxidation

Figure 5.29  Bonding Pad Necks Seen by Breaking Pad with Probe
The actual release time at 35 W power depends on the finger gap in the targeted design variant. Devices with 5 µm finger gap require about 2.5 minutes of release time to completely release thin fingers and to create 0.5 µm necks on bonding pads. Devices with 2.5 µm finger gap require a larger release time between 4 and 6 minutes depending on the size of the isolation neck. While high RF power solves a lot of the problems with the loading effect, it should be noted that the loading effect is still present though in smaller measure. To make the release of the springs less aggressive, the springs are surrounded by blocks of silicon as shown in Figure 5.22. The springs need enough space to twist about the torsional axis for $10^\circ$ – $20^\circ$ motion on either side. While this limits the smallest gap that can be created around the spring and hence the degree of control we have on release loading on the spring, the release is much less aggressive compared to leaving the spring completely open.
5.2.8 Thin Finger and Isolation Neck Through Oxidation

Thermal oxidation is a very predictable process. Sidewall oxidation during various steps in the process does not usually need to be characterized. The oxide thickness is read off from a chart based on the one-dimensional Deal-Grove model. At this step, however, the oxidation process is two-dimensional. The one-dimensional model will not correctly estimate the time required for oxidation fingers and necks through.

For the purpose of characterization, we use the one-dimensional model for an initial indication of oxidation time. The wafer is cleaved into several pieces and all pieces are oxidized for the time indicated by the one-dimensional Deal Grove model. One pieces is taken out of the furnace, the oxide is stripped with BHF and it is examined in the SEM to see if the thinner structures have disappeared. If there are remnants of these structures, the rest of the pieces are oxidized further in steps of 10 minutes. Each time, one more piece is stripped and examined and the oxidation is stopped when the thinner structures have completely disappeared.

Considering 1 µm movable structure width, we need to find the time taken to oxidize 0.5 µm of silicon because the oxidation consumes silicon from both sides of the structures. The release time is calibrated so that necks on wider structures are 1 µm or less in size. With a volume increase factor of 2.27, 0.5 µm silicon oxidizes to 0.5 µm x 2.27 = 1.135 µm of oxide. According to the oxidation chart, it takes 2 hours and 48 minutes to grow 1.135 µm of wet thermal oxide at 1100°C.
We start with a conservative oxidation time of 2 hours and 40 minutes. As expected, oxidation is not complete. The three way intersections on the honeycombs do not have sharp corners and are hence slightly wider than the lines. The two dimensional oxidation of the oxide masked structures gives silicon tips at all the three way intersections in the honey comb structures as shown in Figure 5.31.

It is found that an oxidation time of 3 hours consumes all the silicon in the upper level of the movable structures. Though the comb fingers themselves disappeared even with the 2 hours 40 minutes oxidation, it is possible that the process of etching away the oxide with a BHF dip and then rinsing and drying the device could have blown off a thin remnant of the comb finger. An additional 20 minutes is a reasonable measure of over-oxidation to ensure that the comb fingers and possibly the support structures
too, are fully consumed on the upper level. For this reason, both the honeycomb and the solid mirror devices are oxidized for 3 hours at this step. Figure 5.32 shows the device with the oxide stripped after 3 hour oxidation. Wider structures have a silicon core while thinner structures are etched away.

![Fixed Finger Si Core](image)

Figure 5.32 Top Level Thin Structures Oxidized Through: 3 Hours, Oxide Stripped

For the single mask front side device, all suspended structures including the spring, mirror, actuator arms and moving comb fingers are of the same width. All these structures are hence released during the first level release step. The entire moving structure is attached only at the ends of the spring and is hence compliant both in-plane and out-of-plane. Long thermal oxidation of such a compliant structure creates stress-induced deformation. Oxidation induced stresses are offset to some extent by the fact that oxide flows at the oxidation temperature of 1100°C. However, the volume expansion due to oxidation coupled with the differential thermal coefficients
of silicon and silicon dioxide create stress in the device. The constraints on the ends of the spring serve as the support points when the device buckles under compressive stress. Figure 5.33 shows the warped, released movable structures.

![Image of buckled mirror](image)

Figure 5.33 Buckled Mirror: Long Oxidation of Released Structures

The suspended structures show buckling in multiple directions. We propose the following theory to explain this phenomenon. As the oxidation progresses, a longitudinal compressive stress builds up in the spring. Buckling then occurs in two modes, in-plane and out-of-plane. In-plane buckling probably occurs first because the spring is more compliant in that direction. As the fixed and movable fingers on the comb actuators are spaced very close, in-plane buckling causes the movable fingers to come in contact with the fixed fingers at some point during the oxidation. After this time, the fixed and movable fingers stick to each other thus providing two more
anchors. The two additional anchors cause out-of-plane buckling perpendicular to the spring. The device then buckles in the other direction too. A closer view of the out-of-plane buckling of the spring is shown in Figure 5.34.

![Out-of-Plane Buckling of Torsion Spring](image)

**Figure 5.34  Out-of-Plane Buckling of Torsion Spring**

In-plane buckling of the spring can be more clearly seen in the top view in Figure 5.35. One of the effects of in-plane buckling is the in-plane displacement of movable comb fingers such that the gaps are narrowed and eventually closed. This shifting of fingers is shown in Figure 5.36 with the fingers on the outer edge in contact. Finger shifting is made worse by the lateral volume expansion at the support arms that causes both in-plane and out-of-plane deformation at the interface between the support arms and the comb actuator banks as in Figure 5.37 and Figure 5.38.
Figure 5.35  Released Spring Buckles In-Plane After Thermal Oxidation

Figure 5.36  Finger Shifting After Thermal Oxidation
Figure 5.37 Thermal Oxidation Stress Induced Deformation at Support Arms

Figure 5.38 Stress Induced Deformation at Support Arms: Closer View
For the front side / back side process, all the support structures are the same line width as the fixed fingers. While the first level fixed fingers are released due to lower one-dimension loading during the release step, the support structures are honeycombs and stay attached to the substrate through the isolation neck. The mirror is a solid block and is also attached to the substrate. As a result of this feature, very minor stress effects are seen in the device. There is no in-plane or out-of-plane buckling except for a small deformation that reduces the gap between the innermost comb fingers and the support arms. This deformation is shown in Figure 5.39 where the finger gap is correct everywhere except at the innermost fingers. This problem can potentially be solved by making the innermost short movable finger equal to the width of the fixed finger rather than the other movable fingers. The mask in use does not have devices with the inner fingers modified in this fashion. The change will have to be considered in future versions of the mask.

![Figure 5.39 Slight Buckling on Inner Fingers Reduces Innermost Finger Gap](image-url)
Finger shifting in the front side / back side device is almost non-existent. Figure 5.40 shows a device with 5 \( \mu \text{m} \) finger gap after the 3 hour oxidation run. While the gaps are smaller due to the oxidation, all the gaps are the same. The fact that the movable finger support structures and fixed finger support structures resemble each other exactly ensures that there is no differential change in size. The fact that they are fixed to the substrate also prevents any warping.

![Figure 5.40 Front Side / Back Side Device: No Finger Shifting After Oxidation](image)

An interesting technique was developed to study the two-dimensional stress profile in the oxidation of large released MEMS. The mask pattern was modified to include a mesh of 0.5 \( \mu \text{m} \) lines that anchor the movable structures to the walls. These lines are compliant because their line width is very small and the etch depth is consequently less than the rest of the device because 0.5 \( \mu \text{m} \) lines cannot be etched reliably for large depths. The mesh is also released and keeps the released movable structures from
warping. This means that the mesh, being the weaker structure, deforms to take most of the stress in the device. The deformed mesh after 3 hour thermal oxidation is shown in Figure 5.41.

Figure 5.41 Meshed 0.5 µm Anchors to Study 2-D Stress Profile
The technique could potentially be used as a general method to study complex stresses in MEMS devices. Depending on the deformations observed in the 0.5 µm stress mesh, recommendations could possibly be made to reduce stress induced deformation. While the presence of the mesh itself modifies the stress profile, the method could be used as a good starting approximation since simulations on such large structures will be time consuming.

Bracket design for spring ends was discussed in the previous chapter. The standard U-shaped bracket is not sufficient to take all the stress created by thermal oxidation. The U-shaped bracket deforms after thermal oxidation and is shown in Figure 5.42. The bracket is probably not compliant enough because several devices showed broken springs and broken supports. The “butterfly” shaped bracket is more compliant than the U-shaped bracket along the length of the spring and also does not appreciably affect the static and dynamic characteristics of the device. While this bracket was still not sufficient to resolve stress issues for the single mask front side device, the bracket yielded excellent results for the front side / back side device. Figure 5.43 shows the “butterfly” bracket before thermal oxidation and Figure 5.44 shows the bracket after thermal oxidation. It should be noted that the released spring is still straight when the “butterfly” bracket deforms after oxidation. Additionally there is more room for deformation on the bracket if there are any residual stresses after the device is eventually released and the mask oxide is etched back.
Figure 5.42  Deformation of U-Shaped Bracket After Thermal Oxidation

Figure 5.43  Undeformed “Butterfly” Bracket: Before Long Thermal Oxidation
The vertical isolation segment is oxidized through in the same step if the size of the neck is 1 µm or less. The first level release step is timed to achieve such a neck size. To show vertical isolation a device is cleaved with a probe. Figure 5.45 shows an SEM picture where the silicon cores in the upper and lower levels are less bright compared to the oxide sidewalls and the isolation segment. The picture is not very clear due to the charging effects on the oxide, so an outline has been drawn in an attempt to differentiate silicon and oxide. The isolation segment has been electrically tested after lower level deep Si etch. The remaining mask oxide is etched back on the top. One probe is placed on the fixed finger bonding pad and another probe is placed on the substrate. The DC voltage across the probes is slowly ramped up. It is found that a 0.5 µm neck that oxidizes to about 1.1 µm in width can withstand a voltage of
420 V. Beyond this voltage, sparks can be seen on the bonding pad and the probes are shorted out. The vertical gap between silicon levels is on the order of 5 µm.

![Debris from Cleavage](image)

Figure 5.45 Cleaved Wide Beam: Brightness Difference Shows Vertical Isolation

It has been shown that the single mask front side device is probably not feasible due to the stress effects seen at this stage. We continue with the processing of the front side / back side device at this point because that has larger probability of success. The single mask front side devices, however, are still used for calibration during further process steps. The thermal oxidation step is followed by a long oxide floor clear step to make way for the shadow extension etch to create lower level structures.

5.2.9 Floor Clear

The long thermal oxidation step grows 1.175 µm of oxide on the floor corresponding to 3 hours of wet oxidation at 1100°C. All lines are now wider and gaps are smaller
because of the lateral oxide growth during the oxidation step. The floor is not much
deepener, however. This floor clear step requires a larger over-etch due to the narrow
gaps.

The smallest gap occurs at the innermost comb fingers as shown in Figure 5.39 and
this is the critical gap to watch for floor clear and subsequent lower level Si RIE. It is
found that a floor clear time of 1 hour and 33 minutes is sufficient for clearing the
floor in devices with 5 µm pre-oxidation finger gap. The oxide etch tool etches at a
rate of about 1 µm per hour. At this rate, the working value of over-etch is about 33%.

Devices with smaller gaps are difficult to floor clear reliably at 25 µm depth and it is
even more difficult to extend the etch another 25 µm into silicon because the gaps are
smaller after oxidation. For that reason, further processing steps are designed for
devices that started off with 5 µm finger gaps. Figure 5.46 shows an insufficiently
cleared floor. The smallest gap cannot be etched into the lower level while the other
gaps etch well. As the remaining oxide floor at the smallest gap is very thin, the SF6
etch steps in the subsequent deep Si RIE eventually clear the floor and etch it down.
This creates a silicon step in this gap. It can be seen in Figure 5.46 that the silicon in
the gap is not as tall as the lower level.
5.2.10 Lower Level Deep Silicon RIE

The etch recipe for lower level deep RIE needs to be more aggressive than the first level deep RIE due to the reduced gaps and deeper floors. The first level Bosch recipe is modified for high power to penetrate the smaller and deeper gaps. It is also made more aggressive by increasing the etch step in the deposition-etch cycle from 1 second to 2 seconds. The modified etch step has 15 W RF Power and 2 seconds etch time. Gas flow rates, pressure and other parameters are the same as those in the first deep RIE step. Figure 5.47 shows a device etched with 12 W power and 1 second etch time where the post-oxidation inner finger gap is very small and the gap is barely carried through into the lower level.
Figure 5.47  Inner Finger Gap Barely Carried Through to Lower Level

Figure 5.48  Finger Shifting Causes Lower Level Fingers to Stick
Figure 5.48 shows the lower level of a single mask, front side device where oxidation induced stress effects have caused finger shifting. The end fingers are not attached on the upper level but the upper level gaps are very small. After a lower level deep RIE, the probe station is used to break off the upper level and a more careful examination shows that the end finger gaps close at some point during the lower level etch. The recipe was hence not aggressive enough for the lower level etch.

The 15 W, 2 second etch recipe gives excellent results. Figure 5.49 shows a lower level RIE using this recipe that maintains finger gaps very well. The upper level is again removed with a probe to show the lower level clearly. Inner fingers are shown in Figure 5.50.

![Figure 5.49](image)

**Figure 5.49** Lower Level RIE Maintains Finger Gaps Well

Top Movable Level Removed
The second level deep Si RIE results are demonstrated on single mask front side devices because it is easy to remove the entire movable upper level to look at the lower level in the SEM. The front side / back side devices also produce excellent results with the same recipe. Only the movable comb fingers have fully oxidized upper levels in this case and all support structures have the width of the fixed fingers and are fixed to the substrate. The upper level is strongly attached and it is very difficult to break it off with a probe without getting a lob of debris. Figure 5.51 is an attempt to show the inner finger gap on such a device with a 5 µm starting finger gap. It can be seen that the gap is carried well from the first level to the second level.
Figure 5.51  Inner Gap Copies Well to Lower Level with Aggressive Deep RIE
Front Side / Back Side Device

It is known that the standard Bosch etch process used to etch a straight trench in a wafer will start making a tapering profile if it is not morphed. As the etch progresses, RF power has to be increased and the time in the etch step also has to be increased. The same idea is applied in this case, where the lower level etch parameters have higher power and etch step time compared to the first level etch parameters. The parameters are not continuously morphed, however. The reduction in gap due to oxidation requires a discrete change in recipe parameters from the first to the lower level.

With this step, front side processing is complete. A release step following a further sidewall passivation and floor clear can be timed to release the lower level comb
fingers and not the support structures. Even the wider comb fingers are released because they only have one-dimensional loading. Support structures, the mirror and bonding pads will be attached to the substrate and they have to be released with a back side etch that releases everything but the bonding pads. An optional short thermal oxidation step will protect the bottom portion of all released structures during back side etch.

5.3 Back Side Processing Results

The stencil wafer for back side masking is created by exposing the stencil mask on a wafer with mask oxide. The fiducials on the mask are very carefully aligned to the stepper and the wafer itself is aligned to the screws on the stepper chuck. It is important that the device wafer and the stencil wafer are aligned to the stepper in the same fashion so that aligning these two wafers together will eventually align the front side devices to the back side etch vias.

The stencil mask has a set of large rectangles corresponding to the back side etch vias. The stencil wafer is etched through in the Bosch tool with a thick oxide mask that lasts until most of the wafer is etched. Any vertical etch recipe can be used with a sufficiently long over-etch. A backing wafer needs to be used below the stencil wafer in the Bosch tool so that when the holes in the stencil wafer break through, there is no Helium leak from the back side. The backing wafer need not be bonded. It simply has to be placed beneath the stencil wafer in the load lock. The entire etch takes between 3 and 5 hours depending on the amount of mask oxide used. If thin mask oxide is used, the mask is depleted faster and the etch rate drops once the amount of exposed
silicon increases. The stencil wafer is thin if the mask oxide is thin. An etch hole on the stencil wafer is shown in Figure 5.52.

Figure 5.52 Etch Window on Stencil Wafer

The stencil pattern is transferred to the back side of the device wafer by aligning the flats manually and taping the wafers together. The back side oxide and poly layers are etched on the device wafer using the taped stencil mask. The initial 3 µm mask oxide and the initial 1 µm polysilicon layer go through all the oxidation steps during front side process flow. As a result, part of the poly layer is oxidized and there is an oxide / poly / oxide layer on the back side.

The stencil is then removed and the device wafer is place upside down into the Bosch tool for back side etching. Breakthrough from the back side is detected by the helium leak alarm. Figure 5.53 shows a stencil etch schematic.
On the front side, open areas are etched the deepest. This means that when approaching from the back side, the open areas will show first because the deepest portions have the shortest back side depth. Figure 5.54 shows the first visible signs of breakthrough during back side etch. The areas between the fixed comb finger supports and the bonding pads are the most open and these are seen first. Next, the areas around the spring, supports and mirror are seen. While they are still somewhat enclosed, they are more open than the comb finger gaps and honeycomb gaps. This second stage in the back side etch is shown on Figure 5.55.
Figure 5.54  First Sign of Back Side Breakthrough: Most Open Areas

Figure 5.55  Second Stage of Back Side Breakthrough: Mirror, Spring, Supports
It can be seen that there is always a horizontal and vertical misalignment between the back side vias and the front side devices. That is the reason why breakthrough happens on one side of the device before the other side. The Bosch process inside the back side etch window is never uniform across the window. The center of the window is etched at a slightly faster rate than the edges. If an alignment error causes a certain feature to be closer to the center, the etch non-uniformity causes this feature to be opened up first before a symmetrical copy of that feature opens up on the other side of the device.

![Figure 5.56 Alignment Error in Multiple Comb Bank Device: Back Side](image)

This misalignment issue is highlighted in the dual comb bank device, the back side of which is shown in Figure 5.56 through the etch window. The lower part of the device is closer to the center of the etch window and opens up before the upper part of the device where only one comb bank can be seen at this time. Additionally, the right side
of the device is opening up slower than the left side. This means that there is a pile of silicon still remains at the top right corner even after the bottom left comb actuators and support structures open up completely. Since the back side etch has to be carried on long enough to release all devices, the lower left corner in this case will be over-etched and hence depleted of silicon. The amount of depletion depends on the size of the silicon pile at the top right corner, which in turn is determined by the alignment error. The bigger problem, possibly, is that the mirror is usually close the center of the etch window and is etched the fastest. Lower level silicon in the mirror gets depleted before all the devices are released, thus cutting off the electrical ground path between the movable comb fingers and the spring supports. Figure 5.57 shows the back side etch window as seen from the front side. The etch window is seen only in the more open areas. It is difficult to gauge the extent of release in the comb fingers and honeycombs by looking at the front side.

Figure 5.57 Back Side Etch Window As Seen From Front Side
If the lower level devices on the front side are not released and protected with oxide, the alignment error causes the comb fingers, support structures and the mirror to be depleted of lower level silicon. While movable comb fingers do not have any upper level silicon, fixed comb fingers do. Upper level silicon in the fixed comb fingers is protected by the oxide segment that enables vertical isolation. Lower level silicon is not essential in the fixed comb fingers and their corresponding supports. In fact, the absence of lower level silicon creates an even closer approximation to partial overlap or non-overlapping comb drives. The lower fixed levels need not be grounded any more to remove them from the electrical picture. The lower level of the movable comb fingers is essential, however, to produce Z actuation. It is difficult to selectively release and protect the thin fingers alone when releasing the lower level from the front side. Figure 5.58 shows depleted silicon in the lower level comb fingers as seen from the back side. Only the outline is shown by the sidewall oxide.

Figure 5.58  Lower Level Silicon Depleted on Comb Fingers: Back Side SEM
Figure 5.59  Lower Level of Mirror Just Depleted: Back Side SEM

Figure 5.60  Silicon Slope on Lower Level Supports and Fingers: Back Side SEM
Figure 5.59 and Figure 5.60 show the back side of another device that had better alignment. The device is still unusable though because the lower level of the mirror has just been depleted as can be seen from the micrographs. There is also a small portion of the device that is yet to be released, which means that an additional etch time is required. The etch non-uniformity is shown by the fact that there is a slope in the lower level silicon from the extremities of the comb actuator banks down to the mirror. The mirror and spring supports are closer to the center of the die and are etched the deepest. While the lower level supports on the first set of combs are almost depleted, the outer set of comb fingers and supports are still intact.

One possibility that comes to mind at this point is to stop the back side etch just before the lower level silicon in the mirror is depleted. That would ensure that there is enough silicon in the support structures and the mirror to provide the ground path. The device has to then be released by a long extension etch from the front side as in Figure 5.61. The front side Bosch deep RIE recipe is made even more aggressive by increasing the time in the etch step from 2 seconds to 3 seconds. 15 W RF power is used and deposition time is left at 1 second. Unfortunately, the cumulative effect of high power SF$_6$ etch steps from all the front side process steps depletes mask oxide in the larger structures such as the mirror and later depletes the oxide on the fixed comb fingers and support structures as well. The top level of the mirror and comb fingers is depleted before the back side fully opens up. It is difficult to make the initial mask oxide any thicker because of the low selectivities involved during the resist / poly / oxide pattern transfer. It may be possible to have a larger number of poly and oxide layers to counter this problem but this requires more experimentation with oxide etching. This issue proves the vital importance of mask oxide integrity in SCREAM-like process flows. Figure 5.62 shows the device just after mask oxide is depleted on
the mirror. Comb fingers and support structures start losing mask oxide shortly afterward.

Figure 5.61  Front Side Extension to Release Devices

Figure 5.62  Mask Oxide Depleted on Open Areas Before Comb Fingers
The next process variant involved back etching the device after releasing and protecting the actuators from the front side. Only the comb fingers and open floors can be protected this way. The support structures cannot be released because the honeycomb bonding pads will release simultaneously. The mirror is a large block and cannot be released either. Additionally, a reentrant back side etch with a high RF power of 35 W was used to make the etch windows slightly wider and also to reduce the loading effect in the hope of making the back side floor flatter than before. The wider etch windows are shown in Figure 5.63. They are wide enough to overlap neighboring windows. The raised silicon at the interface between etch windows ensures that the spring supports remain attached to the substrate after release. Figure 5.64 shows the backside SEM of a device that is released from the front side and oxidized. Springs and comb fingers are protected while the mirror and support structures are exposed on the back side.
This process variant achieved an incremental improvement in the back side etch process. The wider etch windows increased the uniformity slightly and the lower level comb fingers and spring were well protected. However, the lower levels of the mirror and support structures were etched away before the device could be released. In combination with a short front side etch, the lower level of the mirror was just etched away before all actuators were exposed. It is useful to note that when the devices were finally released with a combination of front side extension and back side etching, given that there was very little silicon on the upper and lower levels, there was no deformation or warping of the structure, stress related or otherwise.
5.4 Further Ideas for Back Side Release

The back side release process has not been successful so far. The reentrant high power backside window etch and front side release combined with lower level comb finger protection helped the back side process but the mirror and support structures still pose a problem. A few solutions are proposed in this section that might eventually release the back side. The solutions described here are being experimented with and results are not available at the time this thesis is written.

5.4.1 Thicker Mask Oxide

As described earlier, one potential solution is to start the process with thicker mask oxide. The back side etch should stop at the point where the lower level of the mirror is exposed. The lower level device should finally be released with an aggressive front side extension etch. Misaligned etch windows will mean that certain portions of the device are deeper than others. Taller springs will increase the amount of voltage required to actuate the device to a given torsion angle. The device will also have a lower resonance frequency given the larger mass. If this method works, we will nevertheless have a moving micromirror.

5.4.2 KOH Release

Once the mirror is exposed from the back side, a KOH etch might be able to release the device without removing all the silicon from the mirror and support structures. Since KOH stops at the <111> crystal planes, the mirror and support structures might
potentially have faceted sidewalls while their center portions are etched away. This would ensure an electrical path along the sidewalls along with lower mass.

As an alternative to wet KOH etching, profile control was attempted on the Bosch tool to get a tapering profile. Figure 5.65 shows a tapering profile that was intentionally created on the comb fingers using large deposition time and low RF power. While it was possible to achieve this profile on the back side of the mirror with some difficulty, the back side of the support structures still showed depleted silicon like in the previous attempts.

Figure 5.65 Tapering Profile Bosch Recipe: Low Power, Larger Deposition Time
5.4.3 SOI Wafers

SOI wafers with a buried oxide layer at 50 µm will allow a large over-etch from the back side. This method is probably the most tolerant to back side non-uniformities. An additional thin buried oxide layer at 25 µm will achieve vertical isolation with small vertical gap between levels so that the non-overlapping Z comb drive is almost as good as the partial overlap comb drive.

5.4.4 Thin Wafers

As described in the previous chapter, thin wafers can be used for the entire process. Or, the wafer can be thinned down from the back side before patterning the stencil. In the latter case, the front side processing can be done on stronger wafers and thin wafers need to be handled only in the final back side etch stage. Preliminary experiments with very thin wafers show that they are difficult to handle and are extremely fragile. They break especially easily inside etch tools that move these wafers between a loadlock and a chamber. The thinning step is done on the entire back side of the wafer after stripping off the oxide and poly layers. The non-uniformity is spread out across a large area. Subsequent PECVD oxide, stencil patterning and deep Si etching limits the non-uniformity to a shorter etch depth.

An additional advantage in using thin wafers is that if the wafer is made very thin and if the PECVD oxide deposited on the back side after thinning is also very thin, then it might be possible to use an Infra Red microscope to see through the oxide and the silicon simultaneously for back side alignment purposes. While it is possible to see
through the back side before PECVD oxide is deposited as in Figure 5.66, it is still very difficult to do Infra Red based back side alignment through oxide layers.

![Figure 5.66 Infra Red Image of Back Etch Windows and Front Side Devices](image)

Figure 5.66  Infra Red Image of Back Etch Windows and Front Side Devices

Before Backside Breakthrough
5.5 Conclusions

Processing results for the micromirror device were shown in this chapter. Electrical, mechanical and process design results were used to arrive at a set of useful geometries within the performance specifications of the micromirror device. The device had a mirror mounted on a torsional spring. Partial overlap or non-overlapping Z comb actuators were attached to the mirror as they yielded superior performance in the simulations compared to total overlap comb drives in terms of force and range of motion. While most of the processing has been demonstrated, there are problems with back side release of the mirror and actuator supports. Motion of the micromirror device has not yet been demonstrated.

Two parallel process flows are pursued. One is the single mask front side process flow where the mirror appears as a honeycomb structure. The mirror needs to either be filled in with oxide and polished or bonded to a flat mirror at a later stage. All processing was done with a single mask from the front side of the wafer. The process required that all movable structures including the lines on the mirror, movable support structures and movable comb fingers be of the same width. All these structures were released and oxidized through on the first level. A final oxide etch back is necessary to remove the entire top level oxide structure. Long thermal oxidation of the large released structure caused serious stress issues. In-plane and out-of-plane warping caused by buckling effects damaged the device. This process flow was not pursued further because of the stress issues.

The mask oxide in the process needs to be as thick as possible. 3 µm thermal mask oxide was used in the process. Lithography was characterized for 0.5 µm features and
2.5 µm spaces. A thin resist is used for the fine features required by the process. It was shown that an oxide etch based on CHF$_3$ chemistry does not yield straight sidewalls if tuned for high selectivity to photoresist. An intermediate polysilicon layer was used as a hard mask for pattern transfer. High aspect ratio oxide lines were demonstrated by combining a Cl$_2$ / HBr recipe for poly etching and a CHF$_3$ / CF$_4$ recipe for oxide etching.

A custom deep silicon etch was written for smooth sidewalls and high aspect ratio etches that maintain the line width of fine features. It was found that 0.5 µm features were difficult to etch repeatably for large depths. For higher reliability, the rest of the process was targeted at 1 µm movable comb fingers. Smooth sidewalls were obtained by scaling down the deposition and etch times to scale down the scallop size.

A high power release recipe was shown to release honeycomb structures and open structures with minimal loading. The larger vertical height difference between levels created by a high power recipe compared to the more isotropic profile obtained with a low power recipe were compared and the degree of loading was traded off against vertical gap.

The front side / back side devices had continuous solid mirrors and wide line widths on the support structures. This enabled these devices to remain fixed to the substrate during the long thermal oxidation step, thus showing only minimal oxidation related stress effects. The geometry similarity between fixed finger supports and movable finger supports led to similar expansion and contraction of these structures thus almost eliminating finger shifting during oxidation.
Oxide floor clear times were calibrated for loading in small gaps. The lower level structures were demonstrated successfully using deep RIE recipes that were more aggressive than those used for first level structures because of the deeper floors and narrower gaps after thermal oxidation.

Back side release of these devices posed problems in terms of alignment and etch uniformity. Non-zero alignment error led to large asymmetry in the way the back side of the device opened up. As a result, the lower levels of the mirror and the movable support structures were always etched away by the time the device was fully released. Attempts to finish the etch from the front side did not work due to insufficient mask oxide. While the lower level comb fingers could be released from the front side and protected with oxide, the support structures and the mirror were still over-etched. A few techniques were proposed to alleviate the problems with back side etching. Among them were SOI wafers with a buried oxide layer as back side etch stop, wafer thinning to distribute the etch non-uniformity and KOH etching for sidewall faceting of the back sides of the mirror and support structures to provide an electrical path.

Back side etch issues prevented the realization of the micromirror device. Nevertheless, several processing techniques demonstrated here are useful to the processing of 3-D MEMS devices. While the oxidation based multilevel process and the non-overlapping Z comb structures have been designed, simulated and processed, it is hoped that future experiments will be able to solve the back side etch issues to make a moving micromirror device. The next chapter talks about yet another enhancement to the processing of bulk MEMS devices.
References

CHAPTER SIX:
SINGLE CRYSTAL SILICON 3-D WIRE ARRAYS WITH INTEGRATED BULK MEMS

6.1 Abstract

A new process has been developed and demonstrated to create very large three-dimensional arrays of micrometer to nanometer-scale wires [1]. The process in its simplest form requires a single mask and only two processing steps: lithography and etching. A third optional oxidation step is used either to define wires or to control dimensions and material properties. The process can be integrated with bulk MEMS, using one mask. The wires can be made of single crystal silicon, silicon dioxide, or a combination of these with other materials.

6.2 Introduction

Several processes exist in literature to fabricate arrays of wires. Most or all of these processes are used to fabricate two-dimensional nanowire arrays. Materials used include Cadmium Sulfide [2], Ga [3], GaN [4], Boron [6], C_{60} [7], Copper Sulphide [8], Gold [9, 35], Co_{16}Ag_{84}, Bismuth [11, 24, 26, 28, 42], Si [12, 14, 32, 39, 44-46, 51], Antimony [13], Indium [15], Co-Ni [16], Fe_{14}Ni_{86} [17], Co_{67}Ni_{33}, CaF_{2} [19], Indium Oxide [20], Co [21, 25, 29], Ni [22, 40], Fe [23, 27, 30, 34, 36], Silver [33, 48], Copper-Cobalt [38], GaAs/InGaAs [47], SiGe [49], CoSi2 [50] and other metals [5, 31, 37] to name a few. Reported fabrication methods include electron beam
lithography, focused ion beam lithography, deposition / adsorption on surfaces [2-3, 7, 9-10, 13, 15-18, 20-25, 27, 29-30, 34-38, 42], oxidation [5, 32, 39], sputtering [6], gas-vapor-liquid-solid reactions [8, 45], sublimation [44], injection of the melt [11, 26, 28], interferometric lithography [12, 43], ion bombardment [19], electrochemical / electrolytic etching [31, 46], epitaxial growth [47, 50], other self-assembly methods [33, 41, 49] and scanning probe techniques like STM and AFM [48]. Some of these processes do not yield very regular or predictable arrays of wires and all processes require techniques like multiple masking or bonding to extend the array into three dimensions, thus making the process very complex. Serial writing methods are also fairly slow. These processes also do not offer much control over the size of the wires, the gap between the wires or the material.

We propose a controllable process that can create both highly periodic and non-periodic three-dimensional arrays of wires from micron to nanometer dimensions in single crystal silicon with only one mask. A literature survey reveals that this is probably the first and only simple process that can create large 3-D wire arrays. A set of lines on the mask layout is etched into the bulk silicon using an RIE tool running a special wire process. Wires are formed either in this step or in the subsequent thermal oxidation step depending on process design and device requirements. Thermal oxidation is used to define the wires and/or precisely control wire material, size and gap. Wire geometry is controlled by line widths and gaps, the way the lines intersect on the mask, the RIE etch recipe and optional thermal oxidation parameters. The size of the resulting 3-D wire array is determined by the mask layout and processing time on the etching tool. Figure 6.1 shows a 3-D array of wires fabricated using this process. The wires are approximately 100nm in diameter. They are spaced 2 µm apart in plane and 500nm apart out-of-plane.
The wires can be made of pure single crystal silicon, pure silicon dioxide, or a combination of the two. Other materials can be conformally deposited by CVD, sputtering or other methods if required. Several applications have been proposed, including three-dimensional photonic bandgap structures, mechanical coupled oscillators, particle sieves, three-dimensional fluid channel arrays, three-dimensional coupled piezo sensors and three-dimensional arrays of self-aligned lateral tips.

Figure 6.1  Single Mask 3 Dimensional Single Crystal Silicon Wire Array
6.3. The Bosch Process

6.3.1 Introduction

The Bosch process [52] is widely used in the bulk micromachining of silicon. The process is used for rapidly etching vertical profiles in silicon and is highly selective to photoresist and oxide masks. Over the years, it has evolved to perform isotropic silicon release and profile controlled etches. Profile control results in sidewall profiles where the cross-sections vary, within a limited range, with distance into the wafer plane.

The Bosch process works by alternating deposition and etching steps in an Inductively Coupled Plasma (ICP). A passivating material is deposited on the wafer and this is followed by an etching step that etches passivation more aggressively on the floor than on the sides. Once the floor is exposed, the silicon is undercut with an isotropic etch using fluorine chemistry. Rapidly alternating cycles of deposition and etching result in a series of undercuts in silicon, resulting in a profile that is vertical on average. This series of undercuts appear as scallops or ripples on the sidewall. Profile control during etching is achieved by a technique called morphing. Deposition and etch parameters are varied from one cycle to another thus resulting in an etch profile that is different for each cycle. Morphing is used to create cross-sections that are shaped differently from the standard etch profile.

Typical deposition steps are done at 25mTorr with 14sccm C4F8 and 850 watt ICP power for 5 seconds. Typical etch parameters are 25mTorr Pressure, 200 sccm SF6 with 8 watt RIE power and 850 watt ICP power for 7 seconds. Both deposition and
etching steps use backside Helium cooling. Depending on the RIE tool, Argon is optionally used in the plasma.

6.3.2 Effect of Recipe Parameters

Recipe parameters are used to control both the etch rate and the profile of the etch. Larger etch rates are usually achieved by making the process more aggressive by increasing the time in the etch cycle. The deposition cycle time is also increased appropriately so as to maintain the profile shape. The flow rate of the etching gases can also be increased. Profile control is achieved by controlling mainly the RIE electrode power and the etch time relative to the polymer deposition time. Increasing the RIE power makes the etch more anisotropic. Increasing the etch time relative to the deposition time makes the profile more reentrant. Detailed studies have been published on the effect of process parameters on etch rate and cross-sectional profile [53-54]

Figure 6.2 shows a silicon etch with a recipe for a smooth sidewall. Figure 6.3 shows an etch where the recipe has been modified for a rough sidewall. The latter recipes are usually more aggressive with higher etch rates.
Figure 6.2  Bosch Etch for Smooth Sidewalls

Figure 6.3  Bosch Etch for Rough Sidewalls
6.4 The Wire Process

6.4.1 Introduction

The Bosch process results in a naturally rough sidewall profile on Silicon beams. The smoothness of the sidewall can be controlled to an extent using RIE process parameters. Several methods can be used to achieve smoother sidewalls, such as chlorine RIE, replacing the SF6 etch step in the etch deposition cycle with an anisotropic etch step [55], reducing deposition and etch times in cycle in equal proportion and sacrificial oxidation [56]. Thermal oxidation and wet chemical treatments can be used as post etch methods for sidewall smoothening.

While the thrust of most research is on making the sidewall roughness as low as possible, there are advantages in writing processes for intentionally rougher sidewalls. This can be achieved by a combination of several methods. The time in the etch portion of the cycle can be increased relative to the deposition time. This gives deeper undercuts and hence rougher sidewalls. Changing the etch time alone presents the risk of passivation failure on the sidewall before the etch step in the cycle is complete. If there is evidence of sidewall passivation failure, the etch step is made slightly more directional by increasing the RF power at the risk of making the scallops taller in relation to their width. The deposition step already uses zero RIE power and it is difficult to increase lateral deposition by modifying this step. Gas flow rates are found to have a weaker effect on the etch profile compared to cycle times and are hence left at their standard values. Argon flow rate is found to control the stability of the plasma and is increased to stabilize the rapidly alternating etch deposition cycles.
Beyond these modifications, the etch process also needs to be morphed since the etch profile naturally starts to taper in narrow gaps. It is found that in standard etch recipes, line width slowly increases as etching proceeds deeper into the wafer. Morphing ensures that the deposition and etching parameters are increasingly aggressive so as to sustain the etch uniformly across large depths or, equivalently, to ensure that the roughness to line width ratio is maintained throughout the etch. Morphing parameters depend on the width of the gap being etched.

6.4.2 Two Step Wire Process

In one method, wire arrays in three dimensions are formed with only two process steps. A set of lines is exposed on a silicon substrate with photoresist. These lines could be either intersecting or non-intersecting as long as they are attached to a wide support. The exposed lines are etched using a Bosch process where the isotropic undercut during the etch step of the etch deposition cycle is larger than half the line width. In this case the etch time was set to 2.5 times the deposition time. As described earlier, the RF power is increased to ensure that the sidewall passivation is not consumed during the etch. The recipe is morphed so as to increase the RIE power by 1 Watt and the etch time by 2 second every 20 cycles. The result is a consistent array of wires with diamond shaped cross sections into the plane of the wafer as shown in Figure 6.4. The exact recipe and the morphing parameters used are specific to the tool and the pattern layout on the mask. The most significant aspects to pattern layout are the amount of exposed silicon and the trench widths between the lines forming the wires. Smaller trenches need more aggressive etch recipes.
Traditional bulk MEMS layout design dictates that there are no “plus” intersections on the pattern while “T” intersections are allowed. This restriction does not hold for the wire process. In fact, different intersection geometries provide interesting variations on the wire supports after RIE. Figure 6.5 demonstrates the effect of line intersections with a recipe that is aggressive enough to remove the lines but not the intersections. The mask lines and their shadows on the floor can be seen in the picture. Pillars have formed below every intersection while the lines themselves have disappeared.
As the Bosch recipe needs to undercut the lines entirely at every etch step, there is a constraint on the largest line width that can produce wires without destroying sidewall passivation. We have recipes for lines as wide as 2 µm and there is scope for extending the line width further. Of more interest, perhaps, is the smallest size of wires that can be fabricated consistently with this technique. 0.4 µm lines were patterned on photoresist, this being the resolution limit of our stepper. A very aggressive recipe on the RIE tool resulted in severe notching and wires approximately 100nm in diameter as seen in Figure 6.6. Note the 500nm scale on the micrograph. The wire diameter is much smaller than the line width because the Bosch etch naturally starts with a large notching effect that is used to our advantage. The effect of creating this initial undercut is shown on a 1 µm line in Figure 6.7.
Figure 6.6  100 nm Wires from 400nm Lines

Figure 6.7  Initial Notching Reduces Line Width
6.4.3 Three Step Wire Process

Thermal oxidation processes that are normally used to smooth rough surfaces have been used here for achieving quite the opposite effect. If the undercut produced by the etch step on the Bosch cycle is larger than a certain value compared to the line width, subsequent thermal oxidation creates one wire between each set of ripples. Rough etching creates a cross section that is almost diamond shaped but not released. Thermal oxidation effectively separates these silicon segments from each other and connects them with oxide. Stripping the oxide subsequently exposes a 3-D array of released wires. Figure 6.8 shows the process flow for the three step wire process.

![Diagram of 3-D Wire Array by Thermal Oxidation of Rough Surfaces]

Figure 6.8 3-D Wire Array by Thermal Oxidation of Rough Surfaces
The advantage of this method over the two step process is that, if thin wires are required, then oxidizing at an earlier stage makes the process more controllable. Oxidizing wires formed with the two step process will, of course, reduce wire dimensions but more careful timing of the oxidation is required. Thermal oxidation will make the wires prone to higher stress and this is one of the serious drawbacks associated the three step process.

Figure 6.9  Roughness Not Comparable to Line Width.

Lines Smooth Out After Thermal Oxidation

Figure 6.10  Roughness Comparable to Line Width

Sidewall Roughness Oxidizing into Wires

Figures 6.9 and 6.10 show 2D oxidation simulations on Athena/Suprem4 for cases where the sidewall roughness is either small or large compared to the line width.
Wires form when the roughness is large enough. The sidewall scallops in the simulations were also created using Athena. A deposition / etch loop with a small degree of randomness was simulated to show that slight fluctuations in the symmetry of the sidewalls still result in wire formation. The Bosch etch simulation is described in Appendix A.

A notch on a vertical silicon beam has been previously used to fabricate a single wire by thermal oxidation [39]. This process draws on the series of notches naturally created by the Bosch process to create 3-D wire arrays.

A common detail in both the two step and the three step wire process is that the lines that form wires should be of smaller width in the mask pattern. Lines of larger width can be used to form other MEMS structures that can optionally be connected to these wire arrays as described later. Lines of smaller width will either disappear in the etching step or will be consumed entirely in the oxidation step.

6.4.4 Aspect Ratio Control

While the term “wire” is normally used to refer to a released line where the length is much larger than the cross section and the cross section is nearly circular, it might be of interest to create non circular cross sections with aspect ratios larger than one. We define the aspect ratio or the eccentricity as the ratio of the out-of-plane height of the wire to the in plane width.

In the two step process, the RIE power during the etch step can be modified to control the width of each undercut in relation to its height. While maintaining the integrity of
the rest of the recipe in relation to the RIE power, morphing can even be used to create wires of different predetermined aspect ratios along the same line. Aspect ratio control is not as obvious for the three step wire process and we present here an approximate technique to determine wire aspect ratios in relation to etch parameters and oxidation time.

The aspect ratio of the wire depends on the ratio of the lateral undercut to the line width. Unlike in the two step process, there is a range of lateral undercuts possible here for a given line width that will produce wires. This range determines the corresponding range in aspect ratios for the wires. To estimate the aspect ratios, we make the following assumptions for the etching and 2-D oxidation model:

1. The SF$_6$ etch step at each loop is nearly isotropic
2. 2-D thermal oxidation is modeled by propagating wavefronts.

Deviations from assumption 1 will lead to higher aspect ratios. Assumption 2 means that we use a simplified 2-D thermal oxidation model where we only consider boundary shifts due to consumed silicon. Stress effects are ignored and we assume that the oxidation is equidistant from the interface at all times. Figure 6.11 shows a series of gradually increasing ratios of lateral undercut to line width that lead to decreasing aspect ratios after oxidation and hence more “wire” like cross sections.
The results of more such geometric computations are shown in the graph in Figure 6.12. These can be used in process design to arrive at an indication of aspect ratio. Figure 6.18 shows an electron micrograph of a fixed free wire with a high aspect ratio cross section.


6.5 Additional Experimental Results

6.5.1 Mask Patterns

Three different mask layouts were used to produce Fixed-Free, Fixed-Fixed and Lattice-like arrays of wires respectively. Mask patterns are shown in Figures 6.13 and 6.14 along with the wires that are intuitively expected from these patterns. Since “plus” intersections do not etch as well as the lines do, it is reasonable to assume that such intersections will form connecting pillars across the wire stacks in the third dimension.
Figure 6.13  Fixed-Fixed Wires: Mask Pattern
Figure 6.14  Wire Lattice: Mask Pattern
6.5.2 Wire Arrays

Figure 6.15 is an electron micrograph of sidewall ripples on the wall generating an array of released wires on a silicon beam. The wires are spaced about 400nm apart. Figure 6.16 shows an array of wires using a single photoresist mask. A closer view of this array is seen in Figure 6.17. While all of the above wire arrays were made using fixed-fixed mask patterns, Figure 6.18 shows fixed-free wires made using the two step process. Fixed-free wires made using the three step process show severe stress effects and shows signs of breaking apart as in Figure 6.19.

Figure 6.15  Ripples to Wires
Figure 6.16  3-D Wire Array, Photoresist Mask

Figure 6.17  3-D Wire Array Close Up
Figure 6.18  Two Step Fixed Free Wires

Figure 6.19  Fixed Free Wires by Thermal Oxidation: Broken Wires
The loading effect of the Bosch process on these wires has been characterized. Wires were formed using the two step process. Figure 6.20 shows a series of 5 µm spaces that consistently produce five released wires with a given process. With the same process, a large open space is etched more aggressively and produces a larger number of released wires with larger vertical spacing as in Figure 6.21. Though the process goes through the same number of loops in both the open and the closed spaces, more of the wires are released in the open spaces.

Figure 6.20 200nm Wires with 5 µm In-Plane Gaps
Very large consistent 3-D lattices of wires have also been made. Figures 6.22 and 6.23 show a 4000 wire lattice and a 9000 wire lattice respectively.
Figure 6.23  9000 Wire 3-D Lattice

More results are shown with applications in Section 6.7.

6.6 Process Integration with Bulk MEMS

It is very useful to integrate the wire process with standard bulk MEMS processing techniques such as SCREAM [57-58]. We propose a scheme wherein it is possible to integrate bulk MEMS structures with any number of predetermined wires with a SCREAM like process flow, all in one mask. The MEMS structures could either be connected to 3-D wire arrays or could be mechanically isolated.
Figure 6.24  Wire Process Integration with SCREAM MEMS

SCS Wire Process
Rough Beam
2 SCS Wires

Thermal Oxidation
Smoothens Beam & Protects Wires

RIE Oxide Etch
Floor Clear

"Shadow" Extension Etch
Deep RIE
Figure 6.24 (Continued)

Thin Beam Release
Timed SF$_6$ RIE

Passivation
PECVD Oxide

Floor Clear
Oxide RIE

Release
SF$_6$ RIE
The process flow is described in Figure 6.24. Lines that form wires are differentiated from other lines in the pattern by making them of smaller width. Thus the wire process requires a sidewall roughness on the order of the line width, so the width of these “wire forming lines” cannot be large. The pattern is transferred to silicon dioxide and then to the bulk Silicon using the wire process. This process step creates wires out of the thinner lines while leaving rough sidewalls on the wider lines. A subsequent thermal oxidation step either protects the wires or makes wires, if using the 3 step sequence. Thermal oxidation also creates a smooth surface on the wider lines. The floor is then cleared of oxide and etched. The shadow extension of the wires is released with SF$_6$ RIE, generating a partial undercut that notches the wider beams. This step is followed by sidewall passivation, floor oxide clear and release in keeping with standard SCREAM. The result is a MEMS structure integrated with wires all on one chip with only one mask. The electrical isolation technique depends on the specific application. Standard SCREAM isolation by post release metallization will work for simple MEMS devices attached to wires. Oxidized trench isolations [59] as a previous mask level will achieve in-plane electrical isolation with both beam sections and wires. Wire process integration with SCREAM MEMS has not been demonstrated yet and the process flow described here is only a possible schematic.

### 6.7 Applications

The wire process and the results that have been achieved present a wide range of potential applications. A few selected applications are discussed in brief in this section.
6.7.1 3-Dimensional Photonic Bandgap Structures

Figures 6.22 and 6.23 showing the large 3-D arrays of cubic wire lattices provide the possibility of three dimensional photonic bandgap structures. 3-D lattice structures have always been a challenge to make. The most common processing method is to expose one mask of parallel lines for each level, with successive levels at right angles. This process is obviously far more complicated than the wire process for more than a few levels. The wire process, with its inherent simplicity and range of possible geometries, is a prime candidate for 3-D photonic lattices in single crystal silicon, silicon dioxide or other material combinations. It is also a scalable process for creating 3-D lattices and is versatile, with a wide range of possible line widths and spacings.

In-plane wire size and spacing is controlled simply by creating a suitable mask pattern. Out-of-plane size and spacing is controlled using etch parameters, thermal oxidation or material deposition. Thermal oxidation consumes silicon and increases the silicon-silicon gap while decreasing the oxide-oxide gap. Oxidation also creates silicon-oxide material combinations on each wire. Other materials such as metals can be conformally deposited. A typical wire width to pitch ratio of 0.10-0.25 is commonly achieved using this process as shown in several examples in the text. Defects in the lattice structure are easily created, either by removing lines on the mask pattern or by morphing to modify the etch profile. Tunable defects can be made by integrating wire lattices with MEMS actuators as described in Section 6.

Cubic wire lattices have been shown in previous sections. Lattices approaching FCC or diamond structures have been created using hexagonal patterns on the mask instead
of simple square arrays of intersecting wires. Figure 6.25 shows 3-D, diamond like lattices of wires with a silicon waveguide passing through each lattice. The notches on either end can be machined using a focused ion beam tool to create a 45 degree mirror so as to transmit and receive light from the lattice. Figure 6.26 shows closer view of one of these lattices.

Wires become progressively wider as they reach their supports, as seen in Figure 6.17. This results in a series of conical shapes near the supporting structures, while the wires themselves are fairly straight. The wire and its two sloping supports form three faces of a hexagon. But properly tuning the etch recipe and the gaps on the mask pattern, it is possible to make this shape resemble the in-plane hexagon on the mask, thus making the lattice more truly hexagonal. The diamond lattice has hexagonal projections along certain planes but the lines forming these hexagons are not planar. Figure 6.27 and 6.28 show closer views of this lattice, where the cross sectional hexagons are also seen. We have hence demonstrated both cubic and hexagonal 3-D arrays using the same two step process sequence, simply by changing 2-D information on the mask. Figure 6.29 shows a cross sectional view of the lattice after the chip was cleaved.

The existence of 3-D photonic bandgaps with the possible material combinations and within the possible range of geometries allowed by the process needs to be verified.
Figure 6.25  3-D Diamond Like Hexagonal Lattices with Integrated Waveguides
Figure 6.26  Close Up View of Hexagonal Lattice with Integrated Waveguide
Figure 6.27  3-D Wire Arrays: Hexagonal on Both Top View and Cross Section
Figure 6.28  Hexagonal Lattice of Wires

Figure 6.29  Wire Lattice Cleaved with Probe to Show Cross Section
6.7.2 3-Dimensional Fluid Channel Arrays

An interesting variation to the wire process allows the creation of a 3-D array of voids rather than wires. Fluid channel arrays can only be made with the 3 Step process. A very rough etch is performed on narrow trenches such that the roughness is of the order of the trench width. Upon thermal oxidation, each set of scallops closes in to form a void. The profile control feature in the Bosch etcher has been used before to fabricate fluid channels of larger dimensions. Here we combine the sub-micron symmetry produced by scalloping with the wire process on a trench to create large 3-D arrays of voids. These channels are typically under a micron and can be oxidized to nanometer dimensions. Figure 6.30 shows a trench with enhanced ripples oxidizing into an array of channels. Single channels extendable to in-plane 2-D arrays have been previously demonstrated [60]. With good indications from simulations, the feasibility of the 3-D fluid channel array process remains to be demonstrated.

Figure 6.30 High Roughness Trench Oxidizes into 3-D Channel Array
6.7.3 Nanowire Arrays as Low Loss, High Q, High Frequency, Narrow Band Filters

Mechanical filters are used in low loss, high Q and narrow band applications. Mechanical elements can be made to vibrate at high frequency if they are of nanometer dimensions. Arrays of wires reduced to nanometer sizes can potentially be used as mechanical coupled oscillators, coupled in all three dimensions. The frequency characteristics of such arrays need to be studied in detail as the fabrication technology is now available.

6.7.4 Particle Sieves

As mentioned earlier, thermal oxidation is used to reduce wire dimensions and change material properties. Since the oxide also expands the original volume as it grows, thermal oxidation can also be used to reduce the oxide-oxide gap between wires controllably as shown in Figure 6.31.

The loading effect of the etcher, also referred to as ARDE or Aspect Ratio Dependent Etching in the literature, is a well known phenomenon and leads to smaller etch depths in narrower gaps. Since the etch step goes through the same number of deposition-etch cycles in any gap width, the same number of wires will be created in all such trenches. These wires would be spaced farther apart in the larger gaps and would be closer out-of-plane in the smaller gaps due to the difference in etch depths. Figure 6.31 proposes a design for a nanoparticle sieve wherein lateral spacing on the mask translates to out-of-plane spacing between wires that can be controlled very finely by oxidation. Spacing gets progressively smaller from left to right.
Figure 6.31  Thermal Oxidation to Control Gaps for Particle Sieves
6.7.5 Nanowire Arrays as Piezoresistive Elements for Non-Capacitive In-Situ Sensing

Piezoresistive properties of silicon have been demonstrated on single nanowires [61]. The change in resistivity with applied strain can be used for measuring force and displacement without any capacitive elements on chip. A force applied on a wire lattice is distributed among all the wires in the lattice, with each wire feeling a corresponding fraction of that force. To be able to multiply piezoresistive sensing effects, the change in resistivity of each wire must be sensed separately and then summed since any sensing voltage or current is also divided, depending on the lattice. This mandates the need for an electrical isolation scheme between each wire in the array. We are working on such a scheme and we have several more applications in mind that will arise from that scheme if it materializes. Depending on the sensing application, mechanical isolation between array planes by shadow masking may also be of advantage. This application is mentioned here because of the potential advantages of extending single wire piezoresistive sensing to a large array.

6.7.6 3-Dimensional Arrays of Self Aligned Lateral Tips

Figure 6.17 is Section 5.2 shows a close up view of a 3-D wire array. As the wire supports are formed by “T” or “Plus” intersections on the mask pattern, the intersections are etched much less than the wires themselves. The wire becomes progressively wider as it gets close to its support thus forming a conical shape at the support. If the wires are thermally oxidized such that they are just fully consumed, the conical shape at the wall will form a very sharp silicon tip as in Figure 6.32. These large 3-D arrays of tips will be self-aligned in pairs. Two tips formed by the same wire will point at each other.
The process of oxidizing wires ends into tips remains to be proven. Lateral tips can be broken off to make probes for Atomic Force Microscopes. Arrays of field emitters could also potentially be made using these tips.

**6.8 Conclusions and Future work**

The wire process and several variations have been proven and characterized in detail. Wires can be made with one mask and just two steps: lithography and etching, or three steps: lithography, etching and thermal oxidation. The process is repeatable and can create large arrays of fixed-free or fixed-fixed arrays or even large lattices.
interconnected in three dimensions. Thermal oxidation is optionally used to reduce wire dimensions and change gaps between wires. Oxidation is also used to change the material properties of the wire.

The electrical and mechanical properties of these wire arrays need to be characterized in detail. MEMS testing devices need to be built, that characterize these properties for single wires and 2-D and 3-D arrays of wires. Several applications for the wire process have been described including 3-D Photonic Bandgap Structures, piezoresistive sensing, sieves, 3-D fluid channel arrays and mechanical filters. Plenty of work needs to be done to develop these applications to their fullest potential.

Along with the multilevel process, the wires process flow integrated with SCREAM is a unique addition to the short list of processing technologies available for bulk MEMS and nanoscale devices today. This addition opens up a range of exciting possibilities on what MEMS and nanotechnology can create in the future. The next chapter introduces stepping Z actuators, which combines the multilevel and wires process flows. A lower level moving finger made of wires can cause out-of-plane stepping action depending on the geometries used.
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7.1 Summary and Conclusions

The work described in this thesis demonstrated extensions to the processing technologies available for bulk micromachined MEMS devices. While bulk micromachining has unique advantages over surface micromachining, processing of bulk devices still has a long way to go in terms of versatility. The techniques presented in this thesis were a sample of single mask methods to extend processing capabilities and geometries. The multilevel process was demonstrated and used to make Z directional comb drives. While total overlap drives were shown to move, only the design and fabrication of non-overlapping devices were demonstrated. Movement of partial overlap and non-overlapping Z comb drives could not be demonstrated due to problems with back side alignment and release.

The multilevel process used thermal oxidation to translate line width information on the mask into level information. The multiple level process was demonstrated without any alignment requirements or shadow masking and without the use of SOI wafers or wafer bonding. The simplest version of the multilevel process was used to make a moving partial overlap Z actuator.

A combination of the multilevel process with shadow masking yielded an additional level that could be used to make true comb drives for out-of-plane motion with forces resembling ideal in-plane comb actuators. These actuators have a constant force
profile compared to the linear force fall-off for total overlap actuators. They also
double the range of motion of the total overlap actuators for the same device size.
Electrostatic boundary element simulations were used to show resemblance with in-
plane comb drives across several parameters including geometry and voltage. The
simulations showed that the partial overlap feature is a very important requirement for
vertical comb drive structures. Electrical isolation schemes in the same mask were
also described. If comb drives present the ideal means of electrostatic actuation and
capacitive sensing for several in-plane applications then it is possible that the designs
presented in this thesis for Z comb actuators are the ideal drives and sensors for
several out-of-plane applications. The force and displacement characteristics of the
partial overlap and non-overlapping actuators remain to be proven.

A micro-mirror device was designed for a large tilt angle (10°) and large resonance
frequency (50 kHz). Mechanical design issues such as torsional frequency, in-plane
frequency, frequency separation and stress issues were discussed and the device was
designed within the given specifications. Process constraints were applied to restrict
the mechanical design and the mechanical design data was in turn used to design the
process flow. Three different process flows were proposed. The two mask front side
process flow allows independent control of the spring and mirror height and hence
allows flexible tuning of stiffness and mass. A short overlap segment on the device
was shown to greatly improve the starting force of the actuator. The single mask front
side process imposed additional constraints on the line widths to create an electrically
isolated two level actuator, spring and mirror all on the same mask. This process
required an additional step where the top level oxide structures were etched away.
Mask layout was designed to include several geometry variations within the useful
design space.
Stress issues associated with oxidizing released structures on the front side process flow were eliminated to a large extent by attaching the devices to the substrate during long oxidation steps and finally releasing the devices using a backside stencil. The procedure reduced alignment requirements and also eliminated the second lithography step. Potential problems with this approach were also discussed.

The process flow chapter detailed the problems and solutions at each step of the process. Photoresist uniformity was improved using spin ramps, a hard masking layer was used for the oxide pattern transfer and custom Bosch recipes were used for the deep silicon etch steps to achieve faithful pattern transfer while compensating for the loading effect on narrow gaps. Custom release recipes were used to release line widths of interest and to form isolation necks on wider lines. The backside etch recipes were custom built for profile control and reduced curvature. The final device was successfully fabricated except for alignment errors with the backside etch windows for lack of a good alignment tool. Several techniques were discussed, that increased the alignment tolerance.

While the multilevel process is quite complex in nature, the process and characterization results obtained during the research are applicable to a variety of other MEMS devices. The oxidation-etch techniques can be used to make other kinds of 3-D MEMS structures.

The single crystal silicon wire process was demonstrated on several mask patterns and was shown to create large and repeatable 3-D arrays of micron to nanometer scale wires. A two step process was demonstrated, where sidewall scallops caused by deposition-etch cycling were made aggressive enough to release arrays of wires. The
three step wire array process used thermal oxidation to oxidize scallops into wires. Thermal oxidation yielded more controllable wire dimensions, while it also had more serious stress issues, especially with fixed-free wires. A process flow to integrate 3-D wire arrays with SCREAM devices in the same mask was proposed. Among others, the process can potentially be used to fabricate actuators attached to wires. The hexagonal lattice process was demonstrated to create hexagonal cross sections in both top and side views. Several possible applications and variations of the wire process were mentioned.

7.2 Future Work

One distinct thread that ties together the multilevel process and the wire process is a proposed scheme for making stepping actuators in the Z direction. Descriptions of several in-plane stepping actuators are available in literature [1-4]. It can be shown that a comb finger system, as in Figure 7.1 where either the fixed or moving fingers are segmented, has periodic valleys in the force profile as in Figure 7.1. The gaps shown in the fingers correspond to valleys in the force profile. Figure 7.2 shows values of force at various positions. The restoring force of a spring is also overlaid on the plot to show that the valleys still exist even in the presence of the spring.
Figure 7.1  Segmented Fixed Fingers for Stepping Action
If one of the electrodes in the Z actuator can be made of wires, then multiple preferred states would be introduced along the range of motion due to the gaps between the wires. Figure 7.3 shows a stepping Z actuator that uses a combination of the multilevel process and the wire process. The size of the silicon segments and the gaps need to be suitably designed in order to tune the degree of attraction to a certain state and also to ensure stepping action at reasonable voltages.
Figure 7.3  Stepping Z Actuator with Wires and Multilevel Fingers
The multilevel process has extensive potential in the areas of out-of-plane actuation and multi-degree-of-freedom stages. The micro-mirror device needs to be developed to its full potential in terms of high frequency and large angle of twist. Demonstration of scalability using an array architecture on the micro-mirror device will make it more suitable for display and switching applications. The footprint of the device needs to be reduced, possible by placing actuators below the mirror itself. Alternate materials that have large strength should also be examined.

The wire process chapter had a discussion of possible applications. Photonic bandgap devices can potentially be constructed from periodic cubic and hexagonal lattices. Hexagonal lattices are a step closer to face centered cubic and diamond like structures that are sought after in three-dimensional photonics. The potential to introduce lattice defects using process modifications and the ability to attach MEMS actuators to the wires makes this application versatile. 3-D Fluid channel arrays on the nanometer scale will enable applications such as atomization of fluids for micro-engines, and a host of biological applications. Lateral tips can be used as tunneling sensors or for atomic force microscopy. Conical profiles, rather than cylindrical pillars, that oxidize into sharp silicon tips are sought after in the manufacture of scanning microprobes. The other applications such as sieves and coupled oscillators need to be explored.
References


APPENDIX A:

ATHENA SIMULATIONS

Athena was used for simulating several parts of the SCREAM process flow. Athena has modules available for simulating lithography, deposition and etching steps. A limited degree of control is available when programming a process step. For example, an RIE etch step would allow control of the vertical and lateral etch rates and selectivity but would not allow the control of specific process parameters such as gas flow rates, RF power, ICP power and pressure.

Sample Athena programs are shown here. These programs were used at arrive at MEMS structures that could be oxidized to make wires or other multilevel structures.

While the Athena manuals describe the programming language in detail, the various sections shown here have brief comments so as to help understand the program without going into too much detail. Some sections were borrowed from the Athena sample programs.

The program starts with mesh definition and lithography and goes on to demonstrate oxide etching, Bosch deep silicon etching, sidewall passivation, floor clear and release.
# Load Athena Libraries

go athena
#

# SCREAM PROCESS / Mesh Definition and Lithography
#

# Define Illumination System

illumination i.line

illum.filter clear.fil circle sigma=0.5

# define Projection System

projection na=.45

pupil.filter clear.fil circle

# Define Mask

layout lay.clear x.low=-0.50 z.low=-0.5 x.high=0.50 z.high=0.5

# Define Structure and Crystal Plane on Wafer

line x loc=0 spac=0.1

line x loc=0.5 spac=0.05

line x loc=1.0 spac=0.05

line x loc=2.0 spac=0.2

line y loc=0.0 spac=0.02

line y loc=0.5 spac=0.02

line y loc=1.0 spac=0.02

line y loc=5.0 spac=0.02

line y loc=10.0 spac=0.5
init orientation=100

# Deposit CVD Oxide
rate.depo machine=cdv1 oxide a.m cvd dep.rate=1000 step.cov=0.80
deposit machine=cdv1 time=3 minute divis=5

# Define Exposure Parameters for the Dill Exposure Model and Development
# Rate Parameters for the Mack Development Rate Model for the Photoresist “PR”
rate.develop name.resist=PR i.line a.dill=0.83 b.dill=0.03 c.dill=0.016
rmax.mack=0.1 rmin.mack=0.001 mth.mack=0.3 n.mack=5 Dix.0 = 7.55e-13 Dix.E = 3.34e-2

# Define Index of Refraction of User Defined Material “pecvdoxide” as well as
# for the User Defined Photoresist “PR”
optical material=oxide i.line refrac.real=1.50 refrac.imag=5.2
optical photoresist name.resist=PR i.line refrac.real=1.7

# Deposit User Defined Photoresist “PR”
deposit photoresist name.resist=PR thick=1.0 div=45 min.space=0.01

# We now have Substrate+Oxide+PR

# Expose, Develop & Bake
image win.x.lo=-2.0 win.z.lo=0.0 win.x.h=2.0 win.z.h=0.0 dx=0.1 clear n.pupil=2
defocus=0 one.d
expose dose=150
# We now have Substrate+Oxide+Patterned Resist

After lithography, the pattern on the photoresist is transferred into the oxide layer.

# Transfer Pattern into Oxide

rate.etch machine=oxiderieetcher oxide n.m rie directional=100 isotropic=10  
chemical=50.0 divergence=5  
rate.etch machine=oxiderieetcher photoresist n.m rie directional=40 isotropic=4  
chemical=20.0 divergence=2  
etch machine=oxiderieetcher time=5 minute dx.mult=1

# We now have Substrate + Patterned Oxide

# Optionally Strip PR

etch material=PR ALL

The next step is to transfer the pattern from the oxide layer into bulk silicon using a deep silicon etch step. Since the Bosch ICP etcher is commonly used for this step, a deposition etch loop was written with the passivation defined as a custom material.
While passivation is deposited nearly conformally, the etch step etches the floor faster than the sides so as to protect the integrity of the sidewall during each loop.

# Bosch: Loop Passivation and Isotropic Etching

# Define the Deposition Parameters for Passivation
rate.depo machine=deppass material=passivation a.s cvd dep.rate=100
step.cov=0.80

# Define the Etch Parameters
# Silicon SF6 Etch
rate.etch machine=boschsiliconetch rie material=passivation a.s rie directional=300
isotropic=60
rate.etch machine=boschsiliconetch rie silicon u.m rie directional=0 isotropic=1.5
rate.etch machine=boschsiliconetch rie oxide u.m rie directional=0 isotropic=0

# Bosch Deposition Etch Cycle
foreach counter ( 1 to 12 step 1 )
# Deposit Passivation
deposit machine=deppass time=5 seconds divis=5
# Etch Passivation & Silicon with SF6
etch machine=boschsiliconetch time=7 seconds dx.mult=1
end
# For a more realistic etch, add a small random number to deposition time, etch time
# and etch rates so that parameters change slightly from loop to loop
# We Have a MEMS Beam Attached to the Substrate

Finally, the sidewall is passivated with oxide, the floor is cleared and the device is released.

# Deposit Passivation Oxide

rate.depo machine=cvd1 oxide a.m cvd dep.rate=1000 step.cov=0.80
deposit machine=cvd1 time=1 minute divis=5
structure outfile=scream7.str

# Clear oxide on floor with directional RIE etch

rate.etch machine=oxiderieetcher oxide n.m rie directional=100 isotropic=10
chemical=50.0 divergence=5
etch machine=oxiderieetcher time=1 minute dx.mult=0.5

# Release

# Define the Etch Parameters

# Silicon SF6 Etch - Etches Silicon Isotropically

rate.etch machine=boschsiliconetch rie passivation u.m rie directional=0 isotropic=0
rate.etch machine=boschsiliconetch rie silicon u.m rie directional=0 isotropic=1.5
rate.etch machine=boschsiliconetch rie oxide u.m rie directional=0 isotropic=0

# Release SF6 etch

etch machine=boschsiliconetch time=20 seconds dx.mult=1

# Released Bulk Silicon MEMS
Sputtering modules are available if the structures need to be coated with metal. Thermal oxidation is done as a diffusion process. A sample oxidation process is shown below. Stress dependent oxidations are also possible.

```
method fermi compress
diffuse time=20 temp=1050 dryo2
```

Unfortunately, Athena does not seem to have the capability to handle fully released structures that are not attached anywhere in a cross-sectional view.