Integrated Circuits for High Capacity Communications

Mark Rodwell, UCSB
Ultra High-Frequency III-V Transistors:
Aim for 1-2 THz cutoff frequencies
InGaAs/InP bipolar transistors
InGaAs/InP field-effect transistors

Ultra High Frequency III-V ICs
Aim for 500+ GHz digital clock rates
Aim for 700+ GHz amplifiers
other advanced circuits

mm-wave ICs in Silicon
10-160 Gb/s wireless,
mm-wave sensor networks
monolithic arrays for radar & communications

III-V CMOS for Si VLSI
III-V channel MOSFETs for sub-22-nm scaling
-- these will also have THz cutoff frequencies

DARPA TFAST: 200 GHz digital ICs
DARPA SWIFT: THz transistors 340 GHz amplifiers
ONR Contacts: ultra low resistance contacts for THz devices
ONR THz: 150-1000 GHz amplifier ICs
DARPA CHOIR: 20 GHz optical PLLs
DARPA FLARE: 100 GHz op-amps
low noise HBTs

DARPA SMART: 44 GHz InP power amplifiers
44 GHz silicon phased arrays
NSF sensor nets: 60 GHz Si sensor ICs
NSF mm-wave MIMO: 40 Gb/s wireless

SRC: Nonclassical CMOS research center
UCSB / Stanford / Minnesota / UCSD / Massachusetts
THz Transistors are coming soon; both InP & Silicon

InP Bipolars: 250 nm generation: $\rightarrow$ 780 GHz $f_{\text{max}}$, 424 GHz $f_{\tau}$, $\sim$5 V $V_{\text{CEO}}$

125 nm & 62 nm nodes
$\rightarrow$ $\sim$THz devices

IBM IEDM '06: 65 nm SOI CMOS $\rightarrow$ 450 GHz $f_{\text{max}}$, $\sim$1 V operation

Intel Jan '07: 45 nm / high-K / metal gate
(few ML SiO2 @ interface $\rightarrow$ constrains capacitance density)

continued rapid progress
$\rightarrow$ continued pressure on III-V technologies

If you can't beat them, join them!
Will Si MOSFETs will work well at sub-22-nm gate length?
Yes? $\rightarrow$ enables very fast ICs of massive complexity $\rightarrow$ pursue!!
No? $\rightarrow$ investigate InGaAs/InAs/InP channels for CMOS VLSI.
THz InP vs. near-THz CMOS: different opportunities

65 / 45 / 33 / 22 ... nm CMOS
vast #s of very fast transistors
... having low breakdown, high output conductance

what **NEW** mm-wave applications will this enable?

massive monolithic mm-wave arrays
→ 1 Gb/s over ~1 km

mm-wave MIMO

comprehensive equalization of
~100 Gb/s wireless, wireline, optical links
THz InP vs. near-THz CMOS: different opportunities

InP HBT: THz bandwidths, good breakdown, analog precision

340 GHz, 70 mW amplifiers (design)
In future: 700 or 1000 GHz amplifiers?

200 GHz digital logic (design)
In future: 450 GHz clock rate?
→ fast blocks for microwave mixed-signal

25-40 GHz gain-bandwidth op-amps → low IM3 @ 2 GHz
In future: 200 GHz op-amps for low-IM3 10 GHz amplifiers?
We make THz transistors ...  

... by scaling
Frequency Limits and Scaling Laws of (most) Electron Devices

\[ \tau \propto \text{thickness} \]

\[ C \propto \frac{\text{area}}{\text{thickness}} \]

\[ R_{\text{top}} \propto \frac{\rho_{\text{contact}}}{\text{area}} \]

\[ R_{\text{bottom}} \propto \frac{1}{\text{stripe length}} \]

\[ I_{\text{max, space-charge-limit}} \propto \frac{\text{area}}{(\text{thickness})^2} \]

\[ \Delta T \propto \frac{\text{power}}{\text{length}} \times \log \left( \frac{\text{length}}{\text{width}} \right) \]

To double bandwidth,

- reduce thicknesses 2:1
- reduce width 4:1, keep constant length
- current density has increased 4:1

PIN photodiode
InP Bipolar Transistors
### Bipolar Transistor Scaling Laws

**Bipolar Transistor Design**

\[
\begin{align*}
\tau_b & \approx \frac{T_b^2}{2D_n} \\
\tau_c & = \frac{T_c}{2v_{sat}} \\
R_{ex} & = \frac{\rho_{contact}}{A_e} \\
R_{bb} & = \frac{\rho_{sheet}}{12L_e} \left( \frac{W_e + W_{bc}}{6L_e} \right) + \frac{\rho_{contact}}{A_{contacts}} \\
C_{cb} & = \varepsilon A_e / T_c \\
I_{c,Kirk} & \propto v_{sat} A_e (V_{cc,operating} + V_{cc,punch-through}) / T_c^2 \\
\Delta T & \propto \frac{P}{L_e} \left[ 1 + \ln \left( \frac{L_e}{W_e} \right) \right]
\end{align*}
\]

**Changes required to double transistor bandwidth:**

<table>
<thead>
<tr>
<th>parameter</th>
<th>change</th>
</tr>
</thead>
<tbody>
<tr>
<td>collector depletion layer thickness</td>
<td>decrease 2:1</td>
</tr>
<tr>
<td>base thickness</td>
<td>decrease 1.414:1</td>
</tr>
<tr>
<td>emitter junction width</td>
<td>decrease 4:1</td>
</tr>
<tr>
<td>collector junction width</td>
<td>decrease 4:1</td>
</tr>
<tr>
<td>emitter contact resistance</td>
<td>decrease 4:1</td>
</tr>
<tr>
<td>current density</td>
<td>increase 4:1</td>
</tr>
<tr>
<td>base contact resistivity</td>
<td>decrease 4:1</td>
</tr>
</tbody>
</table>

*Linewidths scale as the inverse square of bandwidth because thermal constraints dominate.*
Status of Bipolar Transistors: September 2007

Updated Sept. 2007

$200 \text{ GHz} \quad 300 \text{ GHz} \quad 400 \text{ GHz} \quad 500 \text{ GHz} \quad 600 \text{ GHz} = \sqrt{f_t f_{\text{max}}}$

- Teledyne
- UIUC DHBT
- NTT
- ETHZ/SFU
- UIUC SHBT
- UCSB DHBT
- NGST
- Pohang
- HRL
- IBM SiGe
- Vitesse
256 nm Generation
InP DHBT

150 nm thick collector

4.7 dB Gain at 306 GHz.

70 nm thick collector

f_{\text{max}} = 780 \text{ GHz}
f = 424 \text{ GHz}

50 nm thick collector

f_{\text{max}} = 218 \text{ GHz}
f = 660 \text{ GHz}

340 GHz, 70 mW amplifier design

200 GHz master-slave latch design

Z. Griffith, E. Lind, J. Hacker, M. Jones
### InP Bipolar Transistor Scaling Roadmap

<table>
<thead>
<tr>
<th></th>
<th>Industry</th>
<th>University</th>
<th>University 2007-8</th>
<th>Appears Feasible</th>
<th>Maybe</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Emitter</strong></td>
<td>512</td>
<td>256</td>
<td>128</td>
<td>64</td>
<td>32 nm width</td>
</tr>
<tr>
<td></td>
<td>16</td>
<td>8</td>
<td>4</td>
<td>2</td>
<td>1 $\Omega \cdot \mu m^2$ access $\rho$</td>
</tr>
<tr>
<td><strong>Base</strong></td>
<td>300</td>
<td>175</td>
<td>120</td>
<td>60</td>
<td>30 nm contact width,</td>
</tr>
<tr>
<td></td>
<td>20</td>
<td>10</td>
<td>5</td>
<td>2.5</td>
<td>1.25 $\Omega \cdot \mu m^2$ contact $\rho$</td>
</tr>
<tr>
<td><strong>Collector</strong></td>
<td>150</td>
<td>106</td>
<td>75</td>
<td>53</td>
<td>37.5 nm thick,</td>
</tr>
<tr>
<td></td>
<td>4.5</td>
<td>9</td>
<td>18</td>
<td>36</td>
<td>72 mA/\mu m² current density</td>
</tr>
<tr>
<td></td>
<td>4.9</td>
<td>4</td>
<td>3.3</td>
<td>2.75</td>
<td>2-2.5 V, breakdown</td>
</tr>
<tr>
<td>$f_c$</td>
<td>370</td>
<td>520</td>
<td>730</td>
<td>1000</td>
<td>1400 GHz</td>
</tr>
<tr>
<td>$f_{max}$</td>
<td>490</td>
<td>850</td>
<td>1300</td>
<td>2000</td>
<td>2800 GHz</td>
</tr>
<tr>
<td>Power Amplifiers</td>
<td>245</td>
<td>430</td>
<td>660</td>
<td>1000</td>
<td>1400 GHz</td>
</tr>
<tr>
<td>Digital 2:1 Divider</td>
<td>150</td>
<td>240</td>
<td>330</td>
<td>480</td>
<td>660 GHz</td>
</tr>
</tbody>
</table>
Detection of hazardous chemicals; sensing in low-pressure gas phase
Precise Discrimination: $10^6$ frequency points, $1:10^6$ frequency accuracy, 640-1280 GHz tuning
Fast scanning: $\sim 1$ second for million-frequency-point scan
Field-Effect Transistors...

... both Si and III-V
Simple FET Scaling

Goal double transistor bandwidth when used in any circuit
→ reduce 2:1 all capacitances and all transport delays
→ keep constant all resistances, voltages, currents

If $T_{ox}$ cannot scale with gate length,
$C_{parasitic}/C_{gs}$ increases, ×
g$_m$/W$_g$ does not increase
hence $C_{parasitic}/g_m$ does not scale ×

$C_{gs} \sim \varepsilon W_g L_g / T_{ox}$
$C_{gs,f} \sim C_{gd} \sim \varepsilon W_g$
$C_{sb} \sim C_{db} \sim \varepsilon W_g L_c / T_{sub}$

$\tau \sim L_g / \nu$
g$_m \sim C_{gs} / \tau \sim (\varepsilon L_g W_g / T_{ox}) / \tau$
$G_{ds} \sim C_{d-ch} / \tau \sim \varepsilon W_g / \tau$

If $T_{ox}$ cannot scale with gate length,
$G_{ds}/g_m$ increases ×

S/D contact resistivity reduced 4:1

All lengths, widths, thicknesses reduced 2:1
Well-Known: Si FETs no longer Scale Well

**EOT is not scaling as 1/L<sub>g</sub>**

<table>
<thead>
<tr>
<th>Age (nm)</th>
<th>2.2</th>
<th>2.1</th>
<th>2.0</th>
<th>1.9</th>
<th>1.6</th>
<th>1.5</th>
<th>1.4</th>
<th>1.4</th>
<th>1.3</th>
</tr>
</thead>
<tbody>
<tr>
<td>T&lt;sub&gt;ox&lt;/sub&gt; (mm) [2]</td>
<td>75</td>
<td>65</td>
<td>53</td>
<td>45</td>
<td>37</td>
<td>32</td>
<td>28</td>
<td>25</td>
<td>22</td>
</tr>
<tr>
<td>Gate Length (nm) [2]</td>
<td>47</td>
<td>40</td>
<td>32</td>
<td>30</td>
<td>30</td>
<td>30</td>
<td>30</td>
<td>30</td>
<td>30</td>
</tr>
<tr>
<td>g&lt;sub&gt;m&lt;/sub&gt;/g&lt;sub&gt;ds&lt;/sub&gt; at 5-L&lt;sub&gt;min-digital&lt;/sub&gt; [3]</td>
<td>190</td>
<td>180</td>
<td>160</td>
<td>140</td>
<td>100</td>
<td>90</td>
<td>80</td>
<td>80</td>
<td>70</td>
</tr>
<tr>
<td>1/f-noise (μV&lt;sup&gt;2&lt;/sup&gt;/√Hz) [4]</td>
<td>6</td>
<td>6</td>
<td>6</td>
<td>6</td>
<td>5</td>
<td>5</td>
<td>5</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>σV&lt;sub&gt;th&lt;/sub&gt; matching (mV·μm) [5]</td>
<td>19</td>
<td>15</td>
<td>13</td>
<td>11</td>
<td>9</td>
<td>8</td>
<td>7</td>
<td>6</td>
<td>6</td>
</tr>
<tr>
<td>I&lt;sub&gt;ds&lt;/sub&gt; (μA/μm) [6]</td>
<td>120</td>
<td>140</td>
<td>170</td>
<td>200</td>
<td>240</td>
<td>280</td>
<td>320</td>
<td>360</td>
<td>400</td>
</tr>
<tr>
<td>Peak F&lt;sub&gt;T&lt;/sub&gt; (GHz) [7]</td>
<td>200</td>
<td>220</td>
<td>270</td>
<td>310</td>
<td>370</td>
<td>420</td>
<td>480</td>
<td>530</td>
<td>590</td>
</tr>
</tbody>
</table>

(ITRS roadmap copied from Larry Larson’s files)

High-K gate dielectrics: significant SiO<sub>2</sub> interlayer → limits gate capacitance density

It is also hard to reduce access resistance by the amount needed

**Because gate oxide scales badly, modern MOSFETs scale badly**

output resistance drops, voltage gain drops

gate capacitance does decrease, but other capacitances don't!

... which hurts high-frequency performance
Why consider III-V (InGaAs/InP) CMOS?

Low access resistance: $1 \Omega \cdot \mu m^2$, $10 \Omega \cdot \mu m$

Light electron → high electron velocity
→ increased $I_d/W_g$ at a given oxide thickness (?)
→ decreased $C_{gs}/g_m$ at a given gate length

Challenge:
Low density of states

$$C_{dos} = \frac{q^2 m^*}{\pi \hbar^2}$$

3.4 $\mu F/cm^2$
@ 1 nm EOT
~3 $\mu F/cm^2$
ballistic case

limits $n_s$ to ~ $6 \times 10^{12} /cm^2$
limits $I_d/W_g$
limits $g_m/W_g$

Challenge:
filling of low-mobility satellite valleys

limits $n_s$ to ~ $8 \times 10^{12} /cm^2$
limits $I_d/W_g$

Challenge:
light electron limits vertical scaling
~1.5-2.5 nm minimum
mean electron depth
Drive current simulation - ideal (ballistic) assumptions

22 nm gate length, 5 nm thick InGaAs / InP channel
Circuits & Applications
millimeter-wave...

...Op-Amps
Let's make Audio Power Amplifiers . . . in the GHz!

My 1980 Audio power amp:
10 MHz transistors → 1.5 MHz loop → 36 dB feedback @ 20 kHz → 0.02% distortion

What if we used modern InP transistors?
350 GHz transistors → 50 GHz loop → 26 dB feedback @ 2.5 GHz → very low distortion for 2 GHz (cell phone band etc) amplifiers?

THz transistors → precision analog design at RF & microwave
Reduce distortion with strong negative feedback

- Linear response
- Increasing feedback
- 2-tone intermodulation

R. Eden

**mm-wave Op-Amps for Linear Microwave Amplification**

DARPA / UCSB / Teledyne FLARE: Griffith & Urteaga

**300 GHz / 4 V InP HBT**

Measured 40 GHz bandwidth

Measured 50 dBm OIP3 @ 2 GHz

New designs in fabrication

Simulated 56 dBm OIP3 @ 2 GHz
Microwave Op-Amp

Microwave gains (dB)

<table>
<thead>
<tr>
<th>Frequency (GHz)</th>
<th>$S_{21}$</th>
<th>$S_{11}$</th>
<th>$S_{22}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>20</td>
<td>10</td>
<td>-10</td>
</tr>
<tr>
<td>3</td>
<td>20</td>
<td>10</td>
<td>-10</td>
</tr>
<tr>
<td>4</td>
<td>20</td>
<td>10</td>
<td>-10</td>
</tr>
<tr>
<td>5</td>
<td>20</td>
<td>10</td>
<td>-10</td>
</tr>
</tbody>
</table>

$C_{int} = 200 \text{fF (solid)}, 225 \text{fF (dashed)}, R_{ex2} = 30 \Omega$

K-factor, $|A|

<table>
<thead>
<tr>
<th>Frequency (GHz)</th>
<th>$C_{int}$</th>
<th>$R_{ex2}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>200, 225, 250 fF</td>
<td>30 Ω</td>
</tr>
</tbody>
</table>

Linearity and noise measurements (1.950GHz):

$C_{int} = 200 \text{fF}$, $OIP3 = 51.4 \text{dBm}$, $NF = 6.34 \text{dB}$
A different design (less distortion, more noise)

1.750/1.775 GHz operation
OIP3 / P_{DC} = 416

1.950 / 1.975 GHz operation
OIP3 / P_{DC} = 219

1.750, 1.775GHz operation
\( P_{\text{DC}} = 956 \text{ mW} \)
\( f_{1,2} = 1.750, 1.775 \text{GHz} \)
\( P_{1\text{dB,comp}} = 15.0 \text{ dBm} \)
OIP3, _AVE_ \approx 56 \text{ dBm}

1.950, 1.975GHz operation
\( P_{\text{DC}} = 956 \text{ mW} \)
\( f_{1,2} = 1.950, 1.975 \text{GHz} \)
\( P_{1\text{dB,comp}} = 15.0 \text{ dBm} \)
OIP3, _nom_ = 53.2 dBm
Can we build similar ICs in SiGe?
... or even in 90 / 65 / 45 nm CMOS??

Want to use fast devices,
not thick-oxide pad-driver FETs
**Electronically-Controlled (perhaps Active) Filters**

**Active filters for radio receivers:** dynamic range is a huge problem

At resonance.
Inductor currents increased \( Q:1 \).
Active element current increased \( Q:1 \)
\( Q=100 \rightarrow IP3 \) decreased 40 dB

Below resonance.
Inductor currents = input current.
Active element current = interferer current
filter active again needs high IP3

**Op-amp-based (vs. \( g_m\)-C) filters**
Raw Op-Amp OIP3 might be 60 dBm.
\( Q=10 \rightarrow IP3 \sim 40 \text{ dBm} \)

**Discrete-time filters**
widely tunable
some topologies incur no in-band resonant degradation in IP3
out-of-band currents still are carried by transistor → some impairment in dynamic range
Analog blocks do not fully exploit fast CMOS devices

**source-coupled \( g_m \) blocks:**

\( \times \) incompatible with 1-V operation

**Inverters as \( g_m \) blocks:**

- \( \checkmark \) 1 V operation
- \( \times \) low voltage gain
- \( \times \) low CMRR
- \( \times \) low speed

\[
\frac{1}{f_{\tau,\text{aggregate}}} = \frac{1}{2f_{\tau,\text{NMOS}}} + \frac{1}{2f_{\tau,\text{PMOS}}}
\]

- 133 GHz
- 200 GHz
- 100 GHz

...what is the best approach?

Many better low-voltage differential \( g_m \) blocks...
Active Circuits Synthesized from Fast CMOS Gm blocks

50 Ω resistive feedback amps.  
10 dB, ~60 GHz feasible (45 nm)  
if NMOS-$f_t$-limited

$g_m - Z_t$ broadband amplifiers

$$A_v = g_{m1} \left( R_f - 1 / g_{m2} \right)$$

microwave / mm-wave op-amps  
feedback linearization $\rightarrow$ high IP3  
active filters  
very fast yet precise analog circuits

$g_m = (1 + A_v) / Z_o$  
$R_f = (1 + A_v) \cdot Z_o$
Monolithic millimeter-Wave Arrays
60 GHz Band: Frequency Allocations

Allocations:
57-64 GHz USA
59-63 GHz Europe (tentative)
59-60, 61-66 GHz Japan
Power limit is < 10 W (or more)

Example Channel Allocations for Differential QPSK at 0.8 Hz/bps:
2 GHz for 2.5 Gb/s QPSK
1 GHz for 1.25 Gb/s QPSK

Bandwidth also allocated near 75 GHz for point-point links
millimeter-wave spectrum: new solutions needed

\[ \left( \frac{P_{\text{received}}}{P_{\text{transmit}} } \right) = \left( \frac{1}{16 \pi^2} \right) \left( \frac{\lambda^2}{R^2} \right) e^{-\alpha R} \]

short wavelength → weak signal → short range

highly directional antenna → strong signal → long range

\[ \left( \frac{P_{\text{received}}}{P_{\text{transmit}} } \right) = \left( \frac{D_t D_r}{16 \pi^2} \right) \left( \frac{\lambda^2}{R^2} \right) e^{-\alpha R} \]

narrow beam → must be aimed → no good for mobile

monolithic beam steering arrays → strong signal, steerable

\[ \frac{P_{\text{received}}}{P_{\text{transmit}}} = \frac{N_{\text{receive}} N_{\text{transmit}}}{16} \frac{\lambda^2}{R^2} e^{-\alpha R} \]

32 x 32 array → 60-90 dB increased SNR → vastly increased range

→ multi-Gigabit mobile communications
Row-Column Approach for Large Monolithic Arrays

Row-Column Architecture
1024-element array needs only 64 phase shifters.

Robust mixed-signal design:
- no inductive tuning
- digital LO phase control
- minimal RF propagation

Digital ICs scale, Analog ICs don't

Phase Generation
- tree structure
- varactor-loaded ECL

LO Phase Selection
- ECL

LO distribution
- ECL

RF/IF signal path
- mixed-signal, untuned

first IF  first LO (11 GHz)  2nd IF (~11 GHz)  2nd LO (33 GHz)
Mixed-Signal H-Tree Array: 2nd Approach

Mixed-signal IC design: digital LO, sub-GHz analog IF distribution → compact & robust, scales to large arrays
repetitive structure → rapid & confident design

IBM7HP BiCMOS
millimeter-wave
digital radio...

...at 100+ Gb/s rates
mm-wave MIMO → wireless at 320 Gb/s rates

16 wireless communication links, each channel carrying 4QPSK @ 10 Gb/s
Each channel uses high-gain apertures: ~30 cm diameter, ~40 dB gain
Transmitter is $N \times N$ elements ($N=4$), each transmitting independently
Receiver is $N \times N$ phased array, with beamformer imaging on the $N^2$ transmitters
If element spacings meet Rayleigh criterion, then channels do not interfere

Feasible range exceeds one mile, even in foul weather

Rayleigh Criterion:
Spatial angular separation of adjacent transmitters: $\delta \theta_t = D / R$
Receive array angular resolution: $\delta \theta_r = \lambda / ND$
To resolve adjacent channels, $\delta \theta_r \leq \delta \theta_t \Rightarrow ND = \sqrt{\lambda NR}$
System Theory

- Ideal element spacing allows for complete channel separation
- 2 element channel separation network consists of 90 degree phase shifts

Angular separation of the Tx elements:
\[ \theta_r \approx \frac{D}{R} \]

Angular resolution of the Rx array:
\[ \theta_{res} \approx \frac{\lambda}{n \cdot D} \]

\[ \theta_r \geq \theta_{res} \Rightarrow D = \sqrt{\frac{R \cdot \lambda}{n}} \]
Sensitivity / Range for 320 Gb/s

Use 30 cm paraboloids for individual array elements, use only ~ 3dBm/transmitter

⇒ Adequate SNR for 10 Gb/s/channel at 1km even in bad weather
Millimeter Wave MIMO

- Data rate proportional to the number of TX/RX antenna pairs
- Each channel can support ~10Gbps
- ~20Gbps per antenna element is possible by using cross polarization
  -> 4x4 arrays are capable of 320Gbps
Initial System Design

- Double upconversion BPSK transmitter (3GHz IF)
- Receiver channel separation network at IF, manual tuning
- DPSK demodulator/downconverter
- System architecture decouples channel separation from data demodulation -> carrier recovery not necessary
Outdoor Testing: Frequency Domain Results

- 41m link range
- 1.2Gbps data rate
- Imperfect channel separation on one of the outputs
Outdoor Testing: Time Domain Results

(a) 500ps per division
50mV per division

(b) 500ps per division
50mV per division

<table>
<thead>
<tr>
<th></th>
<th>Channel Number</th>
<th>1</th>
<th>2</th>
</tr>
</thead>
<tbody>
<tr>
<td>BER Single Active Transmitter</td>
<td>&lt;10^{-6}</td>
<td>&lt;10^{-6}</td>
<td></td>
</tr>
<tr>
<td>BER Two Active Transmitters</td>
<td>&lt;10^{-6}</td>
<td>1.8x10^{-6}</td>
<td></td>
</tr>
<tr>
<td>Channel Suppression Ratio (dB)</td>
<td>10Mbps per Channel</td>
<td>27.8</td>
<td>28.8</td>
</tr>
<tr>
<td></td>
<td>600Mbps per Channel</td>
<td>21.1</td>
<td>9.7</td>
</tr>
</tbody>
</table>
Modular System Upgrades

- Migrate channel separation network and data demodulation from IF to baseband
- Upgrade from BPSK to QPSK
- Increase the number of array elements using 60GHz direct conversion chipset
- Implement FPGA based BERT and PRBS generator
- Replace manual channel separation tuning with a control loop
mm-wave MIMO → radio links @ optical speeds
Extensions

MIMO: multiple spatial channels with spatial equalizer

time-division-multiplexed channel: data received with ADC array → multiple spatial channels
channel equalizer has similar form

Architecture generalizes for parallel CMOS implementation of dispersion compensator
→ optical fiber, wireline interconnects, computer backplane interconnects
...in conclusion
THz Transistors will be commonplace

**InP Technologies:**

Multi-THz transistors are feasible.

High Performance per channel: bandwidth, power, linearity

**CMOS:**

billions of transistors, all with 200-500 GHz bandwidth

What can you do with them?

massively parallel communication links
comprehensive equalization of communication channels