Hot Topics and Cool Ideas in Scaled CMOS Analog Design

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Our Research Focus

- High-speed analog and RF circuits
- Device modeling, CAD and test methodology
- Interface circuits for emerging applications
Outline

- Hot topics
  - Design & Modeling Methodology
    - Analog / RF / mm-wave standard cells
  - Test → Scribe-line RF performance screening circuits
  - Circuit → RF front-end, continuous-time equalizer

- Cool ideas
  - Health monitoring silicon

- Summary
Recent Evolution for RF SoC

- 0.25-μm CMOS
- 5-GHz RF transceiver

But difficult to migrate towards 0.13-μm or 90-nm...
Challenges for RF/mm-wave SoC in Scaled CMOS

- High mask cost ($0.5M – $1M)
- Lack of a streamline RF/mm-wave design flow
- Negative impact of technology scaling
  - Device
    - Process variations
    - RF/mm-wave model uncertainty
    - Interconnect parasitic variations
  - Circuit
    - Low voltage headroom due to reduced Vdd

→ Develop a parasitic-aware RF/mm-wave modeling/design methodology
Overcome RF/mm-wave Modeling Uncertainty

- Stand-alone single device model is insufficient
- Accuracy limited by digital RC extraction
- RF/mm-wave model layout ≠ actual circuit layout

- Leverage the insight to optimal RF/mm-wave device layout
- Exploit the modularity of RF/mm-wave circuits at the sub-circuit level

- Design Flexibility
- Model Scalability
- Model Accuracy
- Design Automation

Scalable Analog/RF Sub-Circuit Cells
A Digital-Like Standard Cell Library for RF Design

- Optimized cell library
  - Diff pair, cross-coupled, cascode
  - Inductors and varactors
  - Interconnects
- Parameterized cells (P-Cells)
  - SKILL code based
- Process independent
  - Import design rules from tech files
- Equivalent circuit models

- Assemble like Lego blocks
- Similar to digital standard cell based design flow
Single-Transistor RF Cell Layout

- Folded multi-finger gate
  - Reduce gate resistance
- Dummy poly-silicon gate
  - Reduce mismatch
- Substrate contact ring
  - Substrate resistance
  - Modeling uncertainty
- Highly regular for better manufacturability
  - Includes dummies in the cell template
Parameterized RF/mm-wave Sub-Circuit Cells

- No RC extraction needed within cell boundary
- Each cell has an equivalent circuit model including RC
Cell Test Structures in 0.13-μm CMOS

ACTIVE & PASSIVE DEVICES

INTERCONNECTS

5.0 mm

2.5 mm
Cell-Based RF Design Methodology

Specifications

System-Level Design

RF Circuit Synthesis

RF Sub-Circuit Cell Place & Route

Final Verification

Tapeout / Fab / Chip Testing

Iterations between schematic and layout

Silicon re-spins
RF Performance Screening Using Cell-Based LC Oscillator Array

- LC oscillators with different loadings as process variation monitoring vehicles in scribe-line
- Screening individual parasitic components to identify yield hitters

**Loading Examples**

**Oscillation Frequencies Over PVT Corners**

<table>
<thead>
<tr>
<th>Oscillator Case ID Number</th>
<th>SS @ 110C</th>
<th>TT @ 60C</th>
<th>FF @ 0C</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>7.0 GHz</td>
<td>6.5 GHz</td>
<td>6.0 GHz</td>
</tr>
<tr>
<td>Peak Detector</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{OUT}</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Scribe-Line Oscillator Array Layout and Testing

Zoom in on a single oscillator

During bench testing

Probe1

Moving

Probe2
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UWB (3–5-GHz) RF Front-End

- Integrate the components between antenna and the transceiver
- Key to cost-effective, small form-factor multi-mode or MIMO systems

Down-conversion Mixer

Wideband LNA

Antenna Switch

Matching networks

Chip to board boundary

LO+

GND

LO-

RF+

GND

RF-

IF+

GND

IF-

Vdd

LOdc

RFdc

Vbias

IF

GND

IF

GND

1 mm

1 mm
CMOS T/R Switch with LC-tuned Substrate Bias
UWB LNA with On-Chip Transformer Matching Network

- Input matching $\rightarrow$ source degeneration inductor $\rightarrow$ wide-band transformer
- Operate from 2.8 – 4.8 GHz, draws 6.7 mW from 1.2-V Vdd
- NF $< 4.7$ dB, $S21 > 13.7$ dB, $S11 < –10.4$ dB, $S22 < –13.1$ dB
A 1-V, 3.3-mW, UWB Mixer (Cell-Based)

- Double balanced folded topology
- PMOS LO switches
- Broadband RF choke
- Differential pair, inductor and interconnect sub-circuit cells

Active chip area: 200µmX500µm
High-Speed Adaptive Passive Equalizer

- Passive filter for low-power operation
- Continuous-time (frequency domain) compensation
- No dependency on recovered clock
Tunable Differential Passive Filter

- Broadband input and output matching
- PMOS in triode region for adjustable resistance
- LC components can be low-Q (~3 at 3 GHz)
- Self-resonance frequency > 30 GHz
Channel + Equalizer Frequency Response

Combined response has 8-dB gain difference between dc and 5 GHz

10-dB GC

Equalizer response (for 10 Gbps)

Channel attenuation
20-Gb/s Eye Diagrams Over CAT-5 Cables

**Equalizer Input**

- **2 m (10-dB loss at 10GHz)**

- **5 m (20-dB loss at 10GHz)**

**Equalizer Output**
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Interface Circuits for Structural Health Monitoring Devices

Active Sensing Patch
- Dual sensing and actuation
- Surface-mountable
- Noninvasive and conformable

Power Transmission Inductors
- Near-field magnetic coupling

Wireless Sensor Interface IC
- Actuation and sensing circuits
- Multiplexing of sensor array
- Wireless data transmission
- Rectifier for AC to DC power conversion
Open questions for a wireless power delivery interface

- What is the optimal frequency to use?
- How much power can be transferred wirelessly?
Power Transfer vs. Frequency

-55
-45
-35
-25

-55
-45
-35
-25

10
10^2
10^3
10^4 (MHz)

P_{out}/P_{in} (dB)

No Tissue
With Tissue
Theoretical Limit

Pin
M
on chip
P_{OUT}
Operate at self-resonance as a LC-tank ($Q_{tank} = 11$)

Match $R_{tank}$ to $R_{load}$ for max power

2x3 inductor array

Strapped metals
- No skin effect
- M4 thru RDL
  - 5-µm metal
  - 2.5-µm oxide

- Turns: 13
- Width: 9 µm
- Spacing: 5 µm

$L_s$: 167 nH
$R_s$: 19 Ω
$C_p$: 3.7 pF
Summary

- CMOS scaling offers many research opportunity due to paradigm shifts in design, modeling, and test methodologies
- Higher integration level is needed for multi-mode/MIMO RF front-ends
- Channel equalization become important for >10-Gbps I/Os
- Increasing need for wireless data/power interface circuits for emerging applications