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Researchers Report Highest Performing III-V Metal-Oxide Semiconductor FETs

III-V MOSFETs Promise to Help Deliver Higher Semiconductor Performance at Lower Power Consumption for Next-Generation Servers

viaSemiconductor Research Corporation

Researchers from University of California, Santa Barbara (UCSB) introduced the highest performing III-V metal-oxide semiconductor (MOS) field-effect transistors (FETs) this week at the 2014 Symposium on VLSI Technology.

The UCSB research promises to help deliver higher semiconductor performance at lower power consumption levels for next-generation, high-performance servers. The research is supported by the Semiconductor Research Corporation (SRC), the world?s leading university-research consortium for semiconductors and related te chnologies.

The UCSB team?s III-V MOSFETs, for the first time in the industry, exhibit on-current, off-current and op erating voltage comparable to or exceeding production silicon devices ? while being constructed at small di mensions relevant to the VLSI (very-large-scale integration) industry.

For the past decade, III-V MOSFETs have been widely studied by a large number of research groups, but no research group had reported a III-V MOSFET with a performance equal to, let alone surpassing, that of a silicon MOSFET of similar size. In particular, UCSB?s transistors possess 25 nanometer (nm) gate lengths, an on -current of 0.5mA and off-current of 100nA per micron of transistor width and require only 0.5 volt to operate.

?The goal in developing new transistors is to reach or beat performance goals while making the transistor sm aller?it is no good getting high performance in a big transistor,? saidMark Rodwell, professor of Electrical and Computer Engineering at UCSB. ?In time, the UCSB III-V MOSFET should perform significantly better than si licon FinFETs of equal size.?

To reach this breakthrough in performance, the UCSB team made three key improvements to the III-V MOSFET structure. First, the transistors use extremely thin semiconductor channels, some 2.5nm (17 atoms) thick, with the semiconductor being indium arsenide (InAs). Making such thin layer improves the on-current and reduces the off-current. These ultra-thin layers were developed by UCSB Ph.D student Cheng-Ying Huang under the guidance of ProfessorArthur Gossard.

Next, the UCSB transistors use very-high-quality gate insulators, dielectrics between the gate electrode and the semiconductor. These layers are a stack of alumina (Al_2O_3, on InAs) and zirconia (ZrO_2), and have a very high capacitance density. This means that when the transistor is turned on, a large density of electrons can be induced into the semiconductor channel. Development of these dielectric layers was led by UCSB Ph.D student Varista Chobpattana under the guidance of ProfessorSusanne Stemmer.

Third, the UCSB transistors use a vertical spacer layer design. This vertical spacer more smoothly distributes the field within the transistor, avoiding band-to-band tunneling. As with the very thin InAs channel design, the vertical spacer makes the leakage currents smaller, allowing the transistor's off-current to rival that of silicon MOSFETs. The overall design, construction and testing of the transistor was led by UCSB Ph.D student Sanghoon Lee under Rodwell?s guidance.

?The UCSB team?s result goes a long way toward helping the industry address more efficient computing capa bilities, with higher performance but lower voltage and energy consumption,? said Kwok Ng, Senior Director of Device Sciences at SRC. ?This research is another critical step in helping ensure the continuation of Moore?s Law ? the scaling of electronic components.?