Researchers Demonstrate Controlled Synthesis of Wafer-Scale Bilayer Graphene and High-Performance Transistors

UC Santa Barbara researchers demonstrate ultra-fast and deterministic growth of high-quality and large-area bilayer graphene films with controlled stacking order required for low-power digital electronics.

Researchers at University of California, Santa Barbara, in collaboration with Rice University, have recently demonstrated a rapid synthesis technique for large-area Bernal (or AB) stacked bilayer graphene films that can open up new pathways for digital electronics and transparent conductor applications.

The invention also includes the first demonstration of a bilayer graphene double-gate field-effect transistor (FET), showing record ON/OFF transistor switching ratio and carrier mobility that could drive future ultra-low power and low-cost electronics.

Graphene is the thinnest known (~0.5 nanometer per layer) 2-dimensional atomic crystal. It has attracted wide interest due to its promising electrical and thermal properties and potential applications in electronics and photonics. However, many of those applications are significantly restricted by the zero band gap of graphene that results in leaky transistors not suitable for digital electronics.

In addition to its atomically smooth surfaces, a considerable band gap of up to ~0.25 eV can be opened up in bilayer graphene by creating a potential difference between the two layers, and thereby breaking the inherent symmetry, if the two layers can be aligned along a certain (Bernal or AB) orientation, explained Kaustav Banerjee.
nerjee, professor of electrical and computer engineering and Director of the Nanoelectronics Research Lab at UCSB. "The dual-gated transistors were specifically designed to allow such potential difference to be established between the layers through one of the gates, while the second gate modulated the carriers in the channel," he added. Banerjee's research team also includes UCSB researchers Wei Liu, Stephan Kraemer, Deblina Sarkar, Hong Li and Professor Pulickel Ajayan of Rice University. Their study was recently published in Chemistry of Materials.

The graphene films were grown in a deterministic manner using an engineered bifunctional (Cu:Ni) alloy surface at a relatively low temperature of 920 °C. Large-area (> 3 inch × 3 inch) Bernal (or AB) stacked bilayer graphene growth was demonstrated within few minutes and with nearly 100% area coverage. The bilayer graphene films exhibited electron mobility as high as 3450 cm²/(V·s), which is comparable to that of exfoliated bilayer graphene, thereby confirming very high-quality. The quality of grown graphene was further corroborated by demonstration of high-performance FETs with record ON/OFF ratio that is a key requirement in low-power digital electronics.

"Achieving surface catalytic graphene growth mode and precise control of the surface carbon concentration were key factors for the favorable growth kinetics for AB stacked bilayer graphene," explained Wei Liu, a post-doctoral researcher in Banerjee's group and a co-author of the article. In 2011, Banerjee's group demonstrated a large-area monolayer graphene synthesis method using a copper substrate as catalyst.

Bilayer graphene is close to monolayer graphene in terms of the film thickness with a hexagonal atomic structure and can be derived from its layered bulk form (graphite) in which adjacent layers are held together by relatively weak van der Waals forces. "However, apart from its band gap tunability, bilayer graphene has some key advantages over monolayer graphene. It has higher density of states and suffers much less from interface effects, which are beneficial for improving the current carrying capability," Liu continued.

"This demonstration is very impressive and should have far-reaching implications for the entire 2D materials community," commented Professor Ali Javey, of University of California, Berkeley and a Co-Director of the Bay Area Photovoltaic Consortium (BAPVC).

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