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UCSB-Intel Researchers Propose Cool Solutions for Hot Chips

Optimally-cooled chip operation can be a very effective and practical ?knob? for controlling the increasing powe r dissipation and subsequent thermal problems in high-end integrated circuits (ICs), including microprocessors fabricated using nanometer scale CMOS technologies, according to a group of researchers at the University of California, Santa Barbara and Intel Corporation.

The details of the findings were reported at the 2005 IEEE International Electron Devices meeting in Washington DC December 4-7, by doctoral candidate Sheng-Chih Lin of the Electrical and Computer Engineering (ECE) department and his research advisor Kaustav Banerjee, an associate professor of ECE, along with researchers from Intel?s Advanced Technology Development Lab in Chandler, Arizona, and their Ci rcuit Research Lab, in Hillsboro, Oregon. The paper describing this finding was one of the highlighted articles at this year?s International Electron Devices meeting.

Increasing power dissipation and resulting thermal problems pose a major limitation to our ability to further scale down nanoscale CMOS transistors that form the building blocks of nearly all integrated circuits used in commercial applications.

According to traditional wisdom, lowering the operating temperature via chip cooling improves speed but increases overall cost. Banerjee?s group at UCSB, which focuses on various nanometer scale issues in deeply sc aled CMOS technologies, have been collaborating with key researchers at Intel to understand the tradeoffs between cooling, power dissipation and microprocessor speed. According to their paper in IEDM 2005, lowering the operating temperature in leakage-dominant nanometer scale CMOS technologies can also reduce overall cost since the power needed for cooling may be regained from the lower leakage of the cooled devices.

The paper titled "Analysis and Implications of IC Cooling for Deep Nanometer Scale CMOS Technologies," by Sheng-Chih Lin, Ravi Mahajan, Vivek De and Kaustav Banerjee, explains that while cooling always boosts chip performance, there is actually an optimum temperature beyond which further cooling yields diminishing returns. The article also suggests that Silicon-on-insulator (SOI)-based devices are more responsive to cooling and that the benefits of cooling increase as technology scales -- encouraging news for the industry.

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