Subthreshold CMOS Synapse Arrays with Log-domain 
Conductance-based Dynamics

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Summary: Design and simulation of compact metal-oxide-semiconductor (MOS) transistor designs implementing synapses and neurons are presented for large-scale neuromorphic circuits with high integration density and high-efficiency and applications in brain-like computational tasks.

Recent advances in neuromorphic engineering for brain-like computing and neural prostheses are converging towards realization of electronic synaptic arrays approaching the integration density and energy efficiency of the human brain. A major impediment in this development is the practical realization of complex conductance-based models of biophysical neural and synaptic dynamics in nanoscale electronics.

Here we present highly compact and low-power circuit realizations of conductance-based dynamical models, where each conductance is implemented using a single MOS transistor operating in subthreshold. The dynamic translinear circuits produce linear conductance-based dynamics through a log-domain transformation of voltage variables, exploiting exponential current and capacitance MOS characteristics.

We further present event-addressable neuromorphic arrays with time-multiplexed synaptic input events, pooled by synapse type according to common reversal potential and activation dynamics. One such physical synapse element per postsynaptic neuron is provided for each type, selected by type index along with postsynaptic address. Transistor level simulations validate the linearity of single transistor synaptic and neural conductance dynamics in a 90nm CMOS process.

![Circuit diagram](image)

Fig. 1. a) The circuit implementing the synapse element consisting of 3 MOS transistors. All transistors operate in subthreshold. b) Transistor-level circuit simulation illustrating the log-domain variable \( u \) (top) and time-domain conductance (bottom) corresponding to the activation function \( g(i) \) with 3 groups of different activation widths.